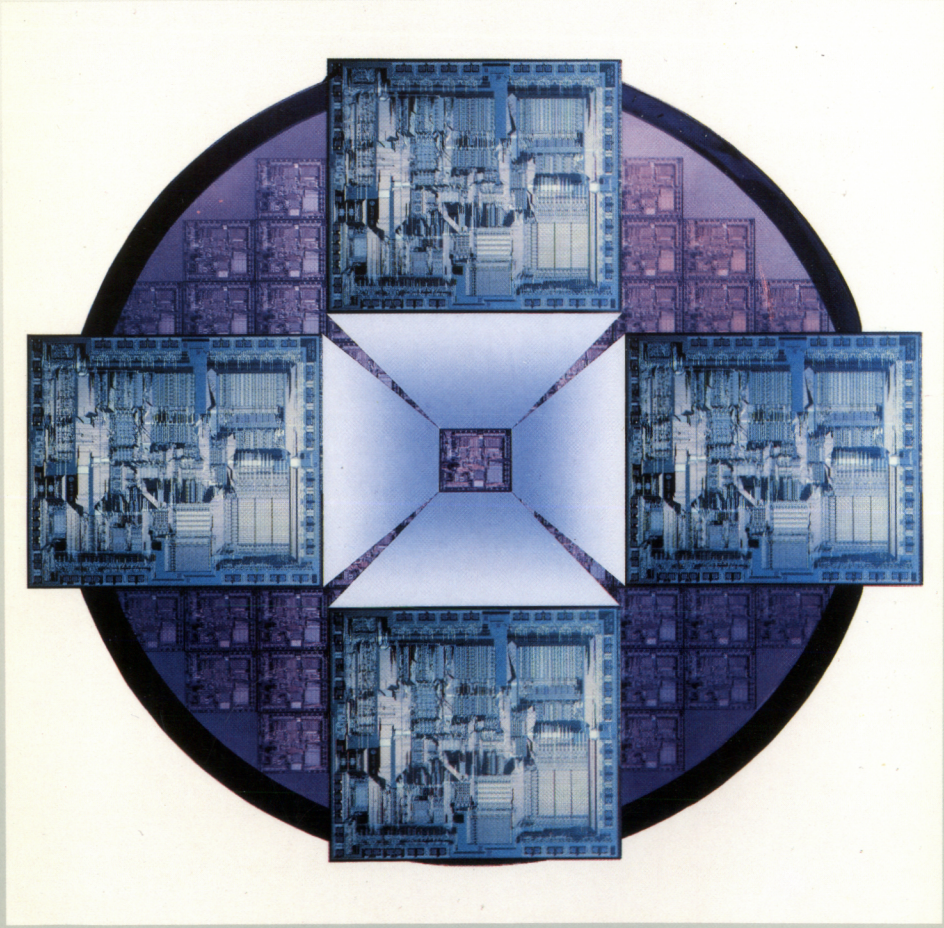
SIEMENS

Microcomputer Components

Microcontrollers

Data Catalog 1988



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Siemens Aktiengesellschaft

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SAB 82C37B	High-performance CMOS programmable DMA controller
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Type Survey for Data Catalog
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Peripheral Components

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SAB 7201A	Multi-protocol serial communications controller
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SAB 8275	Programmable CRT controller
SAB 8276	Small system CRT controller
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SAB 82520/SAF 82520	High-level serial communications controller
SAB 82556	Universal system interface controller, CMOS
SAB 95C60	Quad pixel dataflow manager, CMOS

Memories

SAB 4116-2/-3	RAM, dyn. 16,384 × 1-bit
SAB 41256-10/-12/-15	RAM, dyn., 262,144 × 1-bit
SAB 511000-85/-10/-12	RAM, dyn., CMOS, 1 048,576 × 1-bit
SAB 514256-85/-10/-12	RAM, dyn., CMOS, 262,144 × 4-bit
SAB 81C80	RAM, stat., CMOS, 504 byte

General Information

General Information

Type designation code for ICs

IC type designations are based on the European Pro Electron sytem. The code system is explained in the Pro Electron brochure D 15, edition 1985, available at:

Pro Electron, Avenue Louise, 430 (B. 12)
B-1060 Brussels, Belgium

Mounting instructions

Plastic package

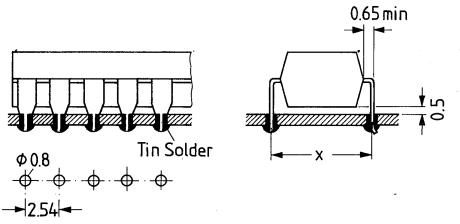
The 90° pins fit into holes with a diameter of 0.7 to 0.9 mm, spaced 2.54 mm apart. See spacing x in figure 1.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for hand soldering and 260°C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 8 s

Storage, pretreatment before processing

The components are to be stored in a dry environment. When solder methods causing solder heat shock stresses are used (reflow soldering where the component is dipped into the solder bath, vapor-phase soldering) it is recommendable to subject IC's in plastic packages to a 24-hour drying phase at 125°C.

Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.
When the pins are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances should the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

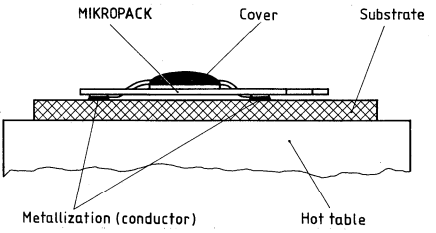
MIKROPACK (SMD)

MIKROPACK components are delivered on film reels.

Mounting suggestions

a) We recommend vapor phase soldering: soldering temperature 215°C, soldering time max. 30 s
b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used (**see figure 2**).

Figure 2



Required equipment and accessories

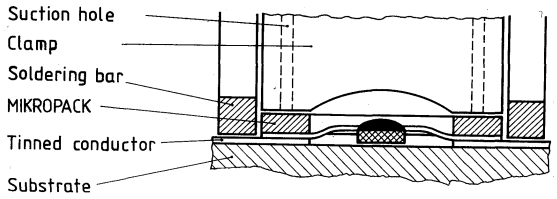
- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6 · · · 40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electro-deposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) bar soldering is also suitable.

Figure 3



Required equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering data

- soldering temperature: 210 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 2 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (**ESS**) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (**ESD**).

Of the multiple of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to $\geq$ 60% and the replacement of highly charging plastics by antistatic materials.
b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of >50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to $10^8\ \Omega$.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) Conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) Anti-static (transparent) tubes.
   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to $10^8\ \Omega$/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are likewise unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control cannot be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting ring.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of $> 40\%$ – this requirement is fulfilled using simple currugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

It must always be ensured that boards do not touch.

In special cases it may be necessary to provide potection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping of our devices, are available from Laber of Munich.

Ultrasonic cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ kHz
exposure	$t < 2$ min
alternating sound pressure	$p < 0.29$ bar
sound power	$N < 0.5$ W/cm^2/liter

Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25\,°C$ and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

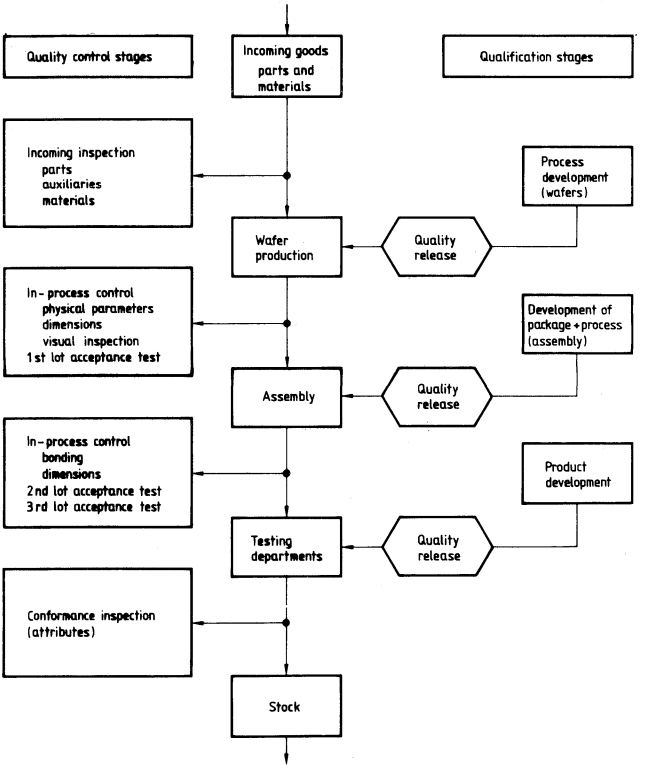
Quality assurance system

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System – Integrated Circuits" (SQS-IC).

Figure 4 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 4



The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
SSI/MSI $\leq$ 1000 gate functions	40	200	100
LSI/VLSI $\geq$ 1000 gate functions	120	400	200

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

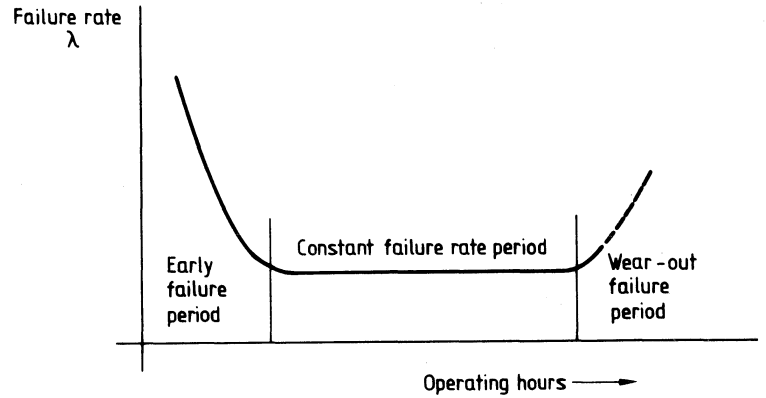
The decreasing failure rates reflect the never ending effort in this direction; they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve (**figure 5**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 5



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp \quad \frac{E_A}{k} \left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 40\,°C$, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Summary of Types (incl. ordering codes)

Summary of Types (incl. ordering codes)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers				
S SAB 8031A-N	Q67120-C271	PL-CC-44	without ROM	59
S SAB 8031A-P	Q67120-C183	P-DIP-40	without ROM	59
SAB 8031A-16-N	Q67120-C349	PL-CC-44	without ROM	59
SAB 8031A-16-P	Q67120-C347	P-DIP-40	without ROM	59
SAB 80C31-N	Q67120-C371	PL-CC-44	without ROM, CMOS	81
SAB 80C31-P	Q67120-C157	P-DIP-40	without ROM, CMOS	81
S SAB 8032A-N	Q67120-C264	PL-CC-44	without ROM	121
S SAB 8032A-P	Q67120-C196	P-DIP-40	without ROM	121
SAB 8032A-16-P	Q67120-C350	P-DIP-40	without ROM	105
SAB 80C32-N	Q67120-C395	PL-CC-44	without ROM, CMOS	141
SAB 80C32-P	Q67120-C378	P-DIP-40	without ROM, CMOS	141
S SAB 8035L-P	Q67120-C43	P-DIP-40	without ROM	39
SAB 8048-P	Q67120-C32	P-DIP-40	1K × 8-bit, ROM	39
SAB 8051A-N	Q67120-C224	PL-CC-44	4K × 8-bit, ROM	59
SAB 8051A-P	Q67120-C186	P-DIP-40	4K × 8-bit, ROM	59
SAB 8051A-16-N	Q67120-C348	PL-CC-44	4K × 8-bit, ROM	59
SAB 8051A-16-P	Q67120-C346	P-DIP-40	4K × 8-bit, ROM	59
SAB 80C51-N	Q67120-C372	PL-CC-44	4K × 8-bit, ROM, CMOS	81
SAB 80C51-P	Q67120-C265	P-DIP-40	4K × 8-bit, ROM, CMOS	81
SAB 8052A-N	Q67120-C263	PL-CC-44	8K × 8-bit, ROM	121

SMD = Surface Mounted Device

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 8052A-P	Q67120-C195	P-DIP-40	8K × 8-bit ROM	121
SAB 80C52-N	Q67120-C396	PL-CC-44	8K × 8-bit ROM, CMOS	141
SAB 80C52-P	Q67120-C379	P-DIP-40	8K × 8-bit ROM, CMOS	141
SAB 80C382	Q67100-H3205	P-DIP-40	without ROM, CMOS	165
SAB 80C382-MP	Q67100-H3242	MIKROPACK	without ROM, CMOS	165
SAB 80C382-PC	Q67100-H3199	Piggyback	without ROM, CMOS	165
SAB 80C382-W	Q67100-H8300	PL-CC-44	without ROM, CMOS	165
SAB 80C482	Q67100-Z154	P-DIP-40	2K × 8-bit ROM, CMOS	165
SAB 80512-N	Q67120-C336	PL-CC-68	4K × 8-bit ROM	195
SAB 80512K-A	Q67120-C333	C-PGA-88	without ROM	219
SAB 80513-N	Q67120-C384	PL-CC-44	16K × 8-bit ROM	247
SAB 80513-P	Q67120-C383	P-DIP-40	16K × 8-bit ROM	247
SAB 80515K-A	Q67120-C267	C-PGA-88	without ROM	299
SAB 80515-N	Q67120-C211	PL-CC-68	8K × 8-bit ROM	267
SAB 80C515-N	Q67120-C297	PL-CC-68	8K × 8-bit ROM, CMOS	333
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SAB 80533-N	Q67120-C386	PL-CC-44	without ROM	247
SAB 80533-P	Q67120-C385	P-DIP-40	without ROM	247
S SAB 80535-N	Q67120-C241	PL-CC-68	without ROM	267
SAB 80C535-N	Q67120-C366	PL-CC-68	without ROM, CMOS	333

SMD = Surface Mounted Device

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers Extended Temperature Range				
SAB 8031A-10-P-T40/110	Q67120-C232	P-DIP-40	−40 to +110°C	389
S SAB 8031A-12-P-T40/85	Q67120-C230	P-DIP-40	−40 to +85°C	389
SAB 80C31-N-T40/85	Q67120-C392	PL-CC-44	−40 to +85°C, CMOS	407
SAB 80C31-P-T40/85	Q67120-C390	P-DIP-40	−40 to +85°C, CMOS	407
SAB 8032A-N-T40/85	Q67120-C367	PL-CC-44	−40 to +85°C	431
S SAB 8032A-P-T40/85	Q67120-C235	P-DIP-40	−40 to +85°C	431
SAB 8032A-P-T40/100	Q67120-C239	P-DIP-40	−40 to +100°C	431
SAB 8035L-P-T40/85	Q67120-C140	P-DIP-40	−40 to +85°C	373
SAB 8048-P-T40/85	Q67120-C133	P-DIP-40	−40 to +85°C	373
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SAB 80C51-P-T40/85	Q67120-C389	P-DIP-40	−40 to +85°C, CMOS	407
SAB 8052A-N-T40/85	Q67120-C368	PL-CC-44	−40 to +85°C	431
SAB 8052A-P-T40/85	Q67120-C247	P-DIP-40	−40 to +85°C	431
SAB 8052A-P-T40/100	Q67120-C248	P-DIP-40	−40 to +100°C	431
SAB 80512-N-T40/85	Q67120-C353	PL-CC-68	−40 to +85°C	195
SAB 80515-N-T40/85	Q67120-C210	PL-CC-68	−40 to +85°C	451
SAB 80515-N-T40/110	Q67120-C316	PL-CC-68	−40 to +110°C	451
SAB 80C515-N-T40/85	Q67120-C388	PL-CC-68	−40 to +85°C, CMOS	333
SAB 80532-N-T40/85	Q67120-C354	PL-CC-68	−40 to +85°C	195
S SAB 80535-N-T40/85	Q67120-C240	PL-CC-68	−40 to +85°C	451
SAB 80535-N-T40/110	Q67120-C313	PL-CC-68	−40 to +110°C	451
SAB 80C535-N-T40/85	Q67120-C387	PL-CC-68	−40 to +85°C, CMOS	333

SMD = Surface Mounted Device

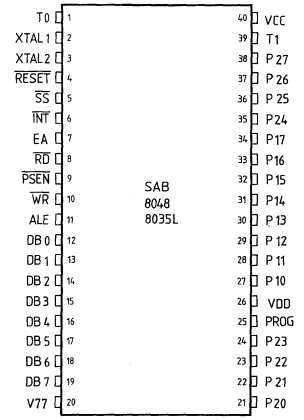
8-Bit Single-Chip Microcontrollers

SAB 8048/8035L
8-Bit Single-Chip Microcontroller

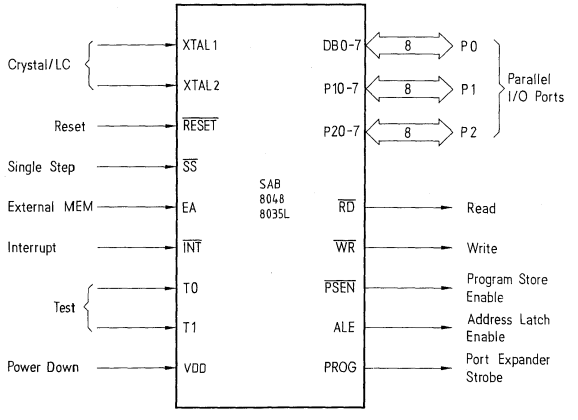
SAB 8048 Microcontroller with factory-maskprogrammable ROM
SAB 8035L Microcontroller for external ROM

- 8-bit CPU, ROM, RAM, I/O in single package
- 8-bit internal timer/event counter
- Instructions 1 or 2 cycles, 2.5 µs or 5.0 µs cycle time
- 96 instructions: 70% single byte
- Compatible with SAB 8080/8085 peripherals
- 1K×8 ROM
  64×8 RAM
  27 I/O lines
- 2 single level interrupts: internal timer/counter and external
- Single +5V supply
- Power-down mode: 15mA standby current for internal RAM

Pin Configuration



Logic Symbol



The SAB 8048/8035L are 8-bit single-chip-microcontrollers implemented in +5 V, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40-pin package. It is 100% compatible with the industry standard 8048.

The SAB 8048 contains a 1K × 8 program memory, a 64×8 RAM data memory, 27 I/O lines and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the SAB 8048 can be expanded using standard memories and SAB 8080/8085 peripherals. The SAB 8035L is the equivalent of an SAB 8048 without program memory and can be used with external ROM and RAM. To minimize development problems and provide maximum flexibility, two pin-compatible versions of this single-chip microcomputer are available: the SAB 8048 with factory-maskprogrammable ROM for low-cost, high-volume production and the SAB 8035 for use with external program memories.

These microcontrollers have extensive bit-handling capabilities as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single-byte instructions and no instructions over 2 bytes in length.

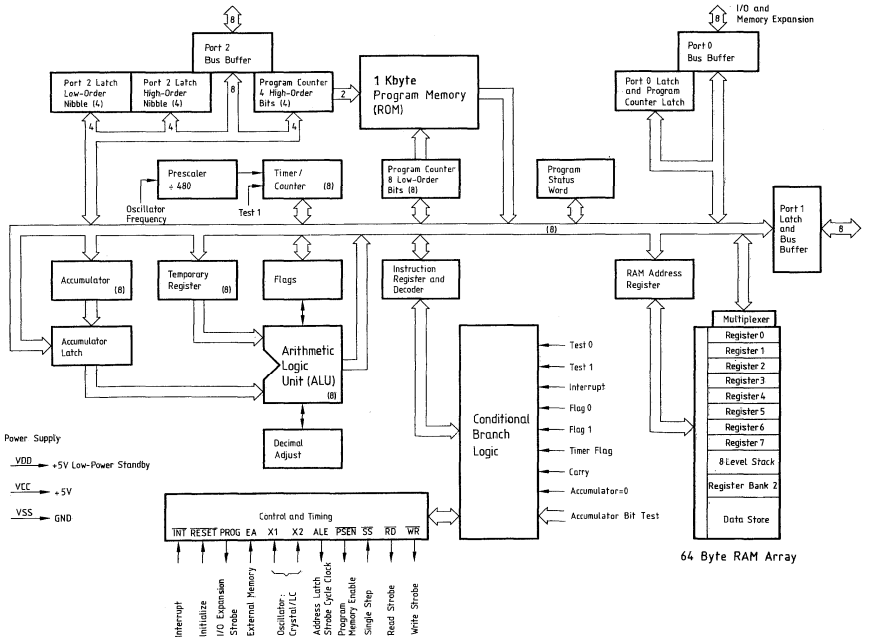
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
T0	1	I/O	TEST PIN 1 Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
XTAL1, XTAL2	2,3	–	OSCILLATOR Inputs for internal oscillator with crystal or external source (non TTL VIH).
$\overline{\text{RESET}}$	4	I	$\overline{\text{RESET}}$ Input which is used to initialize the processor (active low). Also used during power down (non TTL VIH).
$\overline{\text{SS}}$	5	I	$\overline{\text{SINGLE STEP}}$ Can be used in conjunction with ALE to "single step" the processor through each instruction (active low).
$\overline{\text{INT}}$	6	I	$\overline{\text{INTERRUPT}}$ Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (active low).
EA	7	I	EXTERNAL ACCESS Input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (active high).
$\overline{\text{RD}}$	8	O	$\overline{\text{READY}}$ Output strobe activated during a bus read. Can be used to enable data on the bus from an external device. Used as a read strobe to external data memory (active low).
$\overline{\text{PSEN}}$	9	O	$\overline{\text{PROGRAM STORE ENABLE}}$ This output occurs only during a fetch to external program memory (active low).
$\overline{\text{WR}}$	10	O	$\overline{\text{WRITE}}$ Output strobe during a bus write (active low). Used as a write strobe to external data memory.
ALE	11	O	ADDRESS LATCH ENABLE This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
DB0–DB7	12-19	I/O	DATA BUS (0 TO 7) Contains the 8 low-order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{\text{PSEN}}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P20–P27	21-24 35-38	I/O	PARALLEL PORT (20 TO 27) 8-bit quasi-bidirectional I/O port. P20–P23 contain the four high-order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for SAB 8243.
PROG	25	O	PORT EXPANDER STROBE Output strobe for SAB 8243 I/O expander.
P10–P17	27-34	I/O	QUASI-BIDIRECTIONAL PORT 8-bit quasi-bidirectional I/O port.
T1	39	I	TEST PIN 1 Input pin testable using the JT1, and JTN1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
VCC	40		POWER SUPPLY (+5V)
VDD	26		POWER-DOWN VOLTAGE (+5V)
VSS	20		GROUND (0V)

Block Diagram



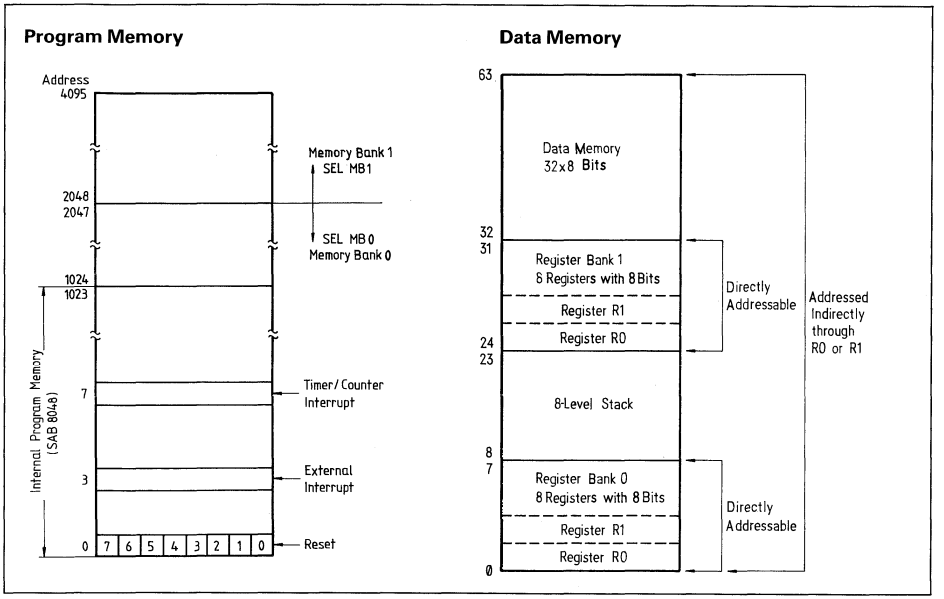
Functional Description

Program Memory

Program memory of SAB 8048 consists of 1024 words 8-bit wide which are addressed by the program counter. Program memory can be used to store constants as well as program instructions. Three locations in program memory are reserved to service the two interrupts (timer/counter and external) and the reset.

Data Memory

Data memory of SAB 8048 is organized as 64 words, 8-bits wide containing the stack and 2 register banks of 8 directly addressable registers.



Timer/Counter

The internal 8-bit binary up-counter can be used to count external events and to generate accurate time delays. The increment from maximum count FF to 00 (overflow) results in the setting of an overflow flag flip-flop and in the generation of interrupt request if the interrupt is enabled.

Depending upon the type of START instruction used the timer/counter is clocked by the oscillator frequency: 480 or an external clock.

The timer/counter is presettable and readable with two MOV instructions.

Interrupts

The two interrupts (timer/counter and external) have the same priority. They can be enabled or disabled under program control.

Input/Output

The SAB 8048 has 27 lines which can be used for I/O functions. These lines are grouped as three 8-bit ports and three test inputs.

Port 1 and 2 are called quasi-bidirectional because each line can serve as an input, an output, or both. Port 0 is a true bidirectional port with associated input and output strobes. Input and output lines on this port cannot be mixed however.

With 4 control and strobe lines, port 0 can be used as a bidirectional bus port to interface external memory and I/O devices. The three pins T0, T1, and $\overline{INT}$ serve as inputs and are testable with conditional jump instructions.

Symbols and Abbreviations

A	Accumulator
AC	Auxillary carry
Addr	12-bit program memory address
An	Accumulator bit n
BS	Bank switch
BUS	Bus port
CY	Carry
CLK	Clock
CNT	Event counter
Data	8-bit number or expression
DBF	Memory bank flip-flop
F0, F1	Flag 0, 1
$\overline{\text{INT}}$	Interrupt
PC	Program counter
PCn	Program counter bit n
Pp	Port 4–7 (for I/O-extension with SAB 8243)
Pr	Port 1 or port 2
PSW	Program status word
Rn	Register bit n
Rr	Register 0–7
SP	Stackpointer
T	Timer
TF	Timer flag
T0, T1	Test 0, test 1
X	Mnemonic for external RAM
#	Immediate data prefix
@	Indirect address prefix
Page	Memory block of 256 byte
( )	Content
→	is moved to
↔	is exchanged with
∧	logical AND
∨	logical OR
⊻	logical EXCLUSIVE OR
–	Complement

Instruction Set Summary

Mnemonic	Function	Description	Hex Code	Flag	Byte	Cycle
Accumulator and register move instructions						
MOV A, Rr	(Rr) → A	Move register contents	F8–FF		1	1
MOV A, @ Rr	((Rr)) → A	Move data memory contents to accumulator	F0–F1		1	1
MOV A, # data	Data → A	Move immediate data data to accumulator	23		2	2
MOV A, PSW	(PSW) → A	Move PSW contents to accumulator	C7		1	1
MOV PSW, A	(A) → PSW	Move accumulator contents to PSW	D7	CY, AC	1	1
MOV Rr, A	(A) → Rr	Move accumulator contents to register	A8–AF		1	1
MOV @ Rr, A	(A) → (Rr)	Move accumulator contents to data memory	A0–A1		1	1
MOV Rr, # data	Data → Rr	Move immediate data to register	B8–BF		2	2
MOV @ Rr, # data	Data → (Rr)	Move immediate data to data memory	B0–B1		2	2
MOVX A, @ Rr	((Rr)) → A	Move external data memory contents to accumulator	80–81		1	2
MOVX @ Rr, A	(A) → (Rr)	Move accumulator contents to external data memory	90–91		1	2
XCH A, Rr	(Rr) ↔ (A)	Exchange accumulator and register contents	28–2F		1	1
XCH A, @ Rr	((Rr)) ↔ (A)	Exchange accumulator and data memory contents	20–21		1	1
XCHD A, @ Rr	((Rr))0–3 ↔ (A)0–3	Exchange accumulator and data memory 4-bit data	30–31		1	1
MOVP3 A, @ A	(PC) save (A) → PC 0–7 011 → PC 8–11 ((PC)) → A PC restor	Move page 3 data to accumulator	E3		1	2
MOVP A, @ A	(PC) save (A) → PC 0–7 ((PC)) → A PC restor	Move current page data to accumulator	A3		1	2
SWAP A	(A) 0–3 ↔ (A) 4–7	Swap nibble within accumulator	47		1	1
Timer/counter move instructions						
MOV A, T	(T) → A	Move timer/counter contents to accumulator	42		1	1
MOV T, A	(A) → T	Move accumulator contents to timer/counter	62		1	1

Instruction Set Summary (cont'd)

Mnemonic	Function	Description	Hex Code	Flag	Byte	Cycle
Port move instructions						
IN A, Pr	(Pr) → A	Input port 1 or 2 data to accumulator	09–0A		1	2
OUTL Pr, A	(A) → Pr	Output accumulator data to port 1 or 2	39–3A		1	2
ANL Pr, # data	(Pr) ∧ data → Pr	Logical AND port 1–2 with immediate mask	99–9A		2	2
ORL Pr, # data	(Pr) ∨ data → Pr	Logical OR port 1–2 with immediate mask	89–8A		2	2
INS A, bus	(bus) → A	Strobed input of bus data to accumulator	08		1	2
OUTL bus, A	(A) → bus	Output accumulator data to bus	02		1	2
ANL bus, # data	(bus) ∧ data → bus	Logical AND bus with immediate mask	98		2	2
ORL bus, # data	(bus) ∨ data → bus	Logical OR bus with immediate mask	88		2	2
MOVD A, PP	(PP) → A0–3 0 → A4–7	Move port 4–7 of SAB 8243 to accumulator Port 4 5 6 7	0C 0D 0E 0F		1 1 1 1	2 2 2 2
MOVD PP, A	(A)0–3 → PP	Move accumulator to port 4–7 of SAB 8243 Port 4 5 6 7	3C 3D 3E 3F		1 1 1 1	2 2 2 2
ANLD PP, A	(A)0–3 ∧ (PP) → PP	Logical AND port 4–7 of SAB 8243 with accumulator mask Port 4 5 6 7	9C 9D 9E 9F		1 1 1 1	2 2 2 2
ORLD PP, A	(A)0–3 ∨ (PP) → PP	Logical OR port 4–7 of SAB 8243 with accumulator mask Port 4 5 6 7	8C 8D 8E 8F		1 1 1 1	2 2 2 2
Arithmetic accumulator instructions						
ADD A, Rr	(A)+(Rr) → A	Add register contents to accumulator	68–6F	AC, CY	1	1
ADD A, @ Rr	(A)+((Rr)) → A	Add data memory contents to accumulator	60 61	AC, CY	1	1
ADD A, # data	(A)+data → A	Add immediate data to accumulator	03	AC, CY	2	2
ADDC A, Rr	(A)+(Rr)+(CY) → A	Add carry and register contents to accumulator	78–7F	AC, CY	1	1
ADDC A, @ Rr	(A)+((Rr))+(CY) → A	Add carry and data memory contents to accumulator	70 71	AC, CY	1	1
ADDC A, # data	(A)+data+(CY) → A	Add carry and immediate data to accumulator	13	AC, CY	2	2

Instruction Set Summary (cont'd)

Mnemonic		Function	Description	Hex Code	Flag	Byte	Cycle
Arithmetic accumulator instructions (cont'd)							
INC	A	(A)+1 → A	Increment accumulator	17		1	1
DEC	A	(A)−1 → A	Decrement accumulator	07		1	1
DA	A		Decimal adjust accumulator	57	AC, CY	1	1
Arithmetic register instructions							
INC	Rr	(Rr)+1 → Rr	Increment register	18–1F		1	1
DEC	Rr	(Rr)−1 → Rr	Decrement register	C8–CF		1	1
INC	@ Rr	((Rr))+1 → (Rr)	Increment data memory location	10–11		1	1
DJNZ	Rr, addr	(Rr)−1 → Rr if (Rr) ≠ 0 Adr → PC0–7	Decrement register and test register if zero	E8–EF		2	2
Logical accumulator and register instructions							
ANL	A, Rr	(A) ∧ (Rr) → A	Logical AND accumulator with register mask	58–5F		1	1
ANL	A, @ Rr	(A) ∧ ((Rr)) → A	Logical AND accumulator with memory mask	50 51		1	1
ANL	A, # data	(A) ∧ data → A	Logical AND accumulator with immediate mask	53		2	2
ORL	A, Rr	(A) ∨ (Rr) → A	Logical OR accumulator with register mask	48–4F		1	1
ORL	A, @ Rr	(A) ∨ ((Rr)) → A	Logical OR accumulator with memory mask	40 41		1	1
ORL	A, # data	(A) ∨ data → A	Logical OR accumulator with immediate mask	43		2	2
XRL	A, Rr	(A) ⊻ (Rr) → A	Logical XOR accumulator with register mask	D8–DF		1	1
XRL	A, @ Rr	(A) ⊻ ((Rr)) → A	Logical XOR accumulator with memory mask	D0 D1		1	1
XRL	A, # data	(A) ⊻ data → A	Logical XOR accumulator with immediate mask	D3		2	2
CLR	A	0 → A	Clear accumulator	27		1	1
CPL	A	$(\overline{A})$ → A	Complement accumulator	37		1	1

Instruction Set Summary (cont'd)

Mnemonic		Function	Description	Hex Code	Flag	Byte	Cycle
Rotate instructions							
RL	A	(An) → An+1	Rotate accumulator left without carry	E7		1	1
RLC	A	(An) → An+1 (A7 → CY (CY) → A0	Rotate accumulator left through carry	F7	CY	1	1
RR	A	(An+1) → An	Rotate accumulator right without carry	77		1	1
RRC	A	(An+1) → An (A0) → CY (CY) → A7	Rotate accumulator right through carry	67	CY	1	1
Flag instructions							
CLR	C	0 → CY	Clear carry bit	97	CY	1	1
CPL	C	$(\overline{CY})$ → CY	Complement carry bit	A7	CY	1	1
CLR	F0	0 → F0	Clear flag 0	85		1	1
CPL	F0	$(\overline{F0})$ → F0	Complement flag 0	95		1	1
CLR	F1	0 → F1	Clear flag 1	A5		1	1
CPL	F1	$(\overline{F1})$ → F1	Complement flag 1	B5		1	1
Branch instructions							
JMP	addr	addr0–7 → PC0–7 addr8–10 → PC8–10 DBF → PC11	Direct jump Page 0 within 2K-block 1 2 3 4 5 6 7	04 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
JMPP	@ A	((A)) → PC0–7	Indirect jump within page	B3		1	2
JC	addr	If (CY) = 1 addr → PC0–7	Jump if carry is set	F6		2	2
JNC	addr	If (CY) = 0 addr → PC0–7	Jump if carry is not set	E6		2	2
JZ	addr	If (A) = 0 addr → PC0–7	Jump if accumulator is zero	C6		2	2
JNZ	addr	If (A) ≠ 0 addr → PC0–7	Jump if accumulator is not zero	96		2	2
JT0	addr	If T0 = 1 addr → PC0–7	Jump if test 0 is high	36		2	2

Instruction Set Summary (cont'd)

Mnemonic		Function	Description	Hex Code	Flag	Byte	Cycle
Branch instructions (cont'd)							
JNT0	addr	If T0 = 0 addr → PC0–7	Jump if test 0 is low	26		2	2
JT1	addr	If T1 = 1 addr → PC0–7	Jump if test 1 is high	56		2	2
JNT1	addr	If T1 = 0 addr → PC0–7	Jump if test 1 is low	46		2	2
JF0	addr	If F0 = 1 addr → PC0–7	Jump if flag 0 is set	B6		2	2
JF1	addr	If F1 = 1 addr → PC0–7	Jump if flag 1 is set	76		2	2
JTF	addr	If TF = 1 addr → PC0–7 0 → TF	Jump if timer flag is set	16	TF	2	2
JNI	addr	If $\overline{INT}$ = 0 addr → PC0–7	Jump if interrupt input is low	86		2	2
JBn	addr	If bit n = 1 addr → PC0–7	Jump if accumulator bit n is set n = 0 1 2 3 4 5 6 7	 12 32 52 72 92 B2 D2 F2		 2 2 2 2 2 2 2 2	 2 2 2 2 2 2 2 2
Subroutine instructions							
CALL	addr	(PC0–11,PSW) → (SP) (SP)+1 → SP addr0–7 → PC0–7 addr8–10 → PC8–10 DBF → PC11	Subroutine call Page 0 1 2 3 4 5 6 7	 14 34 54 74 94 B4 D4 F4		 2 2 2 2 2 2 2 2	 2 2 2 2 2 2 2 2
RET		(SP)–1 → SP ((SP)) → PC	Return without PSW restore	83		1	2
RETR		(SP)–1 → SP ((SP)) → PC ((SP)) → PSW4–7	Return with PSW restore	93	AC, CY	1	2

Instruction Set Summary (cont'd)

Mnemonic	Function	Description	Hex Code	Flag	Byte	Cycle
Control instructions						
STRT T		Start timer	55		1	1
STRT CNT		Start event counter	45		1	1
STOP TCNT		Stop timer/event-counter	65		1	1
EN TCNTI		Enable timer/counter interrupt	25		1	1
DIS TCNTI		Disable timer/counter interrupt	35		1	1
EN I		Enable external interrupt	05		1	1
DIS I		Disable external interrupt	15		1	1
SEL RB0	0 → BS	Select register bank 0	C5		1	1
SEL RB1	1 → BS	Select register bank 1	D5		1	1
SEL MB0	0 → DBF	Select memory bank 0	E5		1	1
SEL MB1	1 → DBF	Select memory bank 1	F5		1	1
ENT0 CLK		Enable clock output	75		1	1
NOP		The NOP instruction	00		1	1

Absolute Maximum Ratings*

Ambient temperature under bias	0 to + 70°C
Storage temperature	−65 to +125°C
Voltage on any pin with respect to ground	−0.5 to + 7 V
Power dissipation	1.5 W

DC Characteristics

TA = 0 – 70°C; VCC = VDD = +5V ±10%; VSS = 0V

Symbol	Parameter	Limit values			Unit	Test Conditions
		min.	typ.	max.		
VIL	Input low voltage (all except $\overline{RESET}$, XTAL1, XTAL2)	−0.5	–	0.8	V	–
VIL1	Input low voltage ($\overline{RESET}$, XTAL1, XTAL2)	−0.5	–	0.6	V	–
VIH	Input high voltage (all except XTAL1, XTAL2, $\overline{RESET}$)	2.0	–	VCC	V	–
VIH1	Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	3.8	–	VCC	V	–
VOL	Output low voltage (BUS)	–	–	0.45	V	IOL = 2.0 mA
VOL1	Output low voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	–	–	0.45	V	IOL = 1.8 mA
VOL2	Output low voltage (PROG)	–	–	0.45	V	IOL = 1.0 mA
VOL3	Output low voltage (all other outputs)	–	–	0.45	V	IOL = 1.6 mA
VOH	Output high voltage (BUS)	2.4	–	–	V	IOH = 400 µA
VOH1	Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4	–	–	V	IOH = 100 µA
VOH2	Output high voltage (all other outputs)	2.4	–	–	V	IOH = 40 µA
IL1	Input leakage current (T1, $\overline{INT}$)	–	–	±10	µA	VSS ≤ VIN ≤ VCC
ILI1	Input leakage current (P10–P17, P20–P27, EA, $\overline{SS}$)	–	–	−500	µA	VSS + 0.45 ≤ VIN ≤ VCC
ILO	Output leakage current (BUS, TO) (high impedance state)	–	–	±10	µA	VSS + 0.45 ≤ VIN ≤ VCC
IDD	VDD supply current	–	5	15	mA	–
IDD+ ICC	Total supply current	–	60	135	mA	–

* Stresses above those listed under "Absolute Maximum Ratings" may cause irreversible damage to the device. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

AC Characteristics

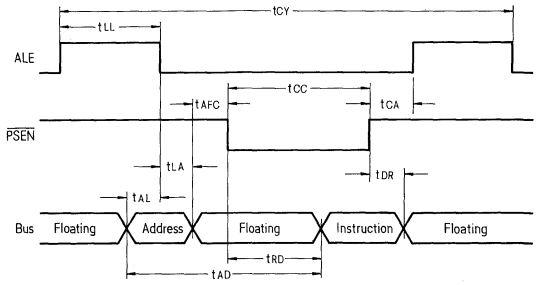
TA = 0 to 70°C; VCC = VDD = 5 V ± 10%; VSS = 0 V

Symbol	Parameter	Limit Values		Unit	Test Conditions *
		min.	max.		
tLL	ALE pulse width	400	–	ns	–
tAL	Address setup to ALE	120	–	ns	–
tLA	Address hold from ALE	80	–	ns	–
tCC	Control pulse width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700	–	ns	–
tDW	Data setup before $\overline{WR}$	500	–	ns	–
tWD	Data hold after $\overline{WR}$	120	–	ns	CL = 20 pF
tCY	Cycle time	2.5	15.0	µs	6 MHz crystal = 2.5 µs
tDR	Data hold	0	200	ns	–
tRD	$\overline{PSEN}$, $\overline{RD}$ to data in	–	500	ns	–
tAW	Address setup to $\overline{WR}$	230	–	ns	–
tAD	Address setup to data in	–	950	ns	–
tAFC	Address float to $\overline{RD}$, $\overline{PSEN}$	0	–	ns	–
tCA	Control pulse to ALE	10	–	ns	–

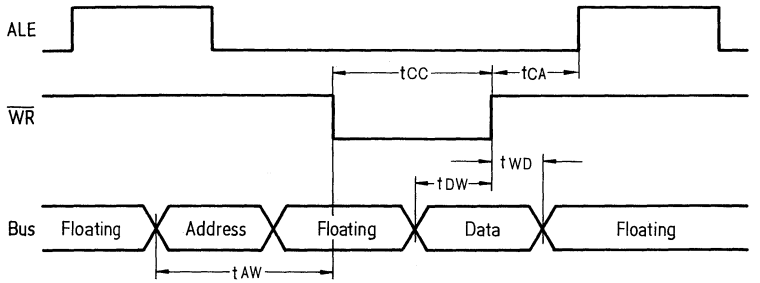
* Control outputs: CL = 80 pF; BUS outputs: CL = 150 pF

Waveforms

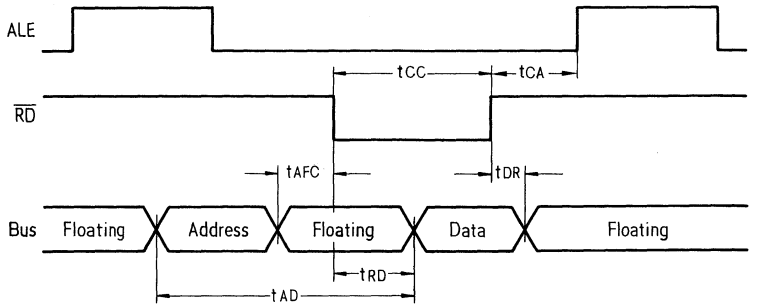
Instruction fetch from external program memory



Read From External Data Memory



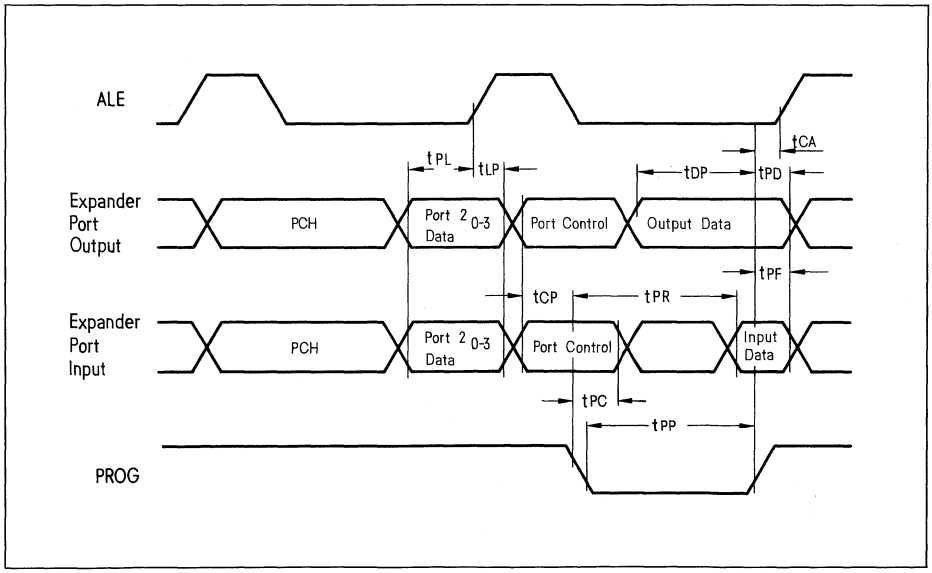
Write to External Data Memory



AC Characteristics (Port 2 Timing)

TA = 0 to 70°C; VCC = VDD = 5 V ±10%; VSS = 0 V

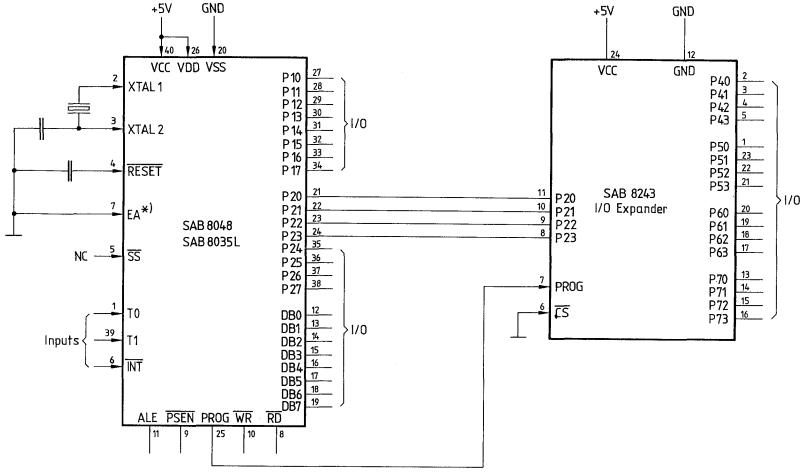
Symbol	Parameter	Limit Values		Unit
		min.	max.	
tCP	Port control setup before falling edge of PROG	110	–	ns
tPC	Port control hold after falling edge of PROG	100	–	ns
tPR	PROG to time P2 input must be valid	–	810	ns
tPF	Input data hold time	0	150	ns
tDP	Output data setup time	250	–	ns
tPD	Output data hold time	65	–	ns
tPP	PROG pulse width	1200	–	ns
tPL	Port 2 I/O data setup	350	–	ns
tLP	Port 2 I/O data hold	150	–	ns



I/O Expansion with I/O Expander SAB 8243

The SAB 8243 is an input/output expander designed specifically for the SAB 8048 family. The I/O ports of the SAB 8243 serve as a direct extension of the SAB 8048 ports and can be addressed by own instructions.

Adding the SAB 8243 I/O expander to the SAB 8048/8035L

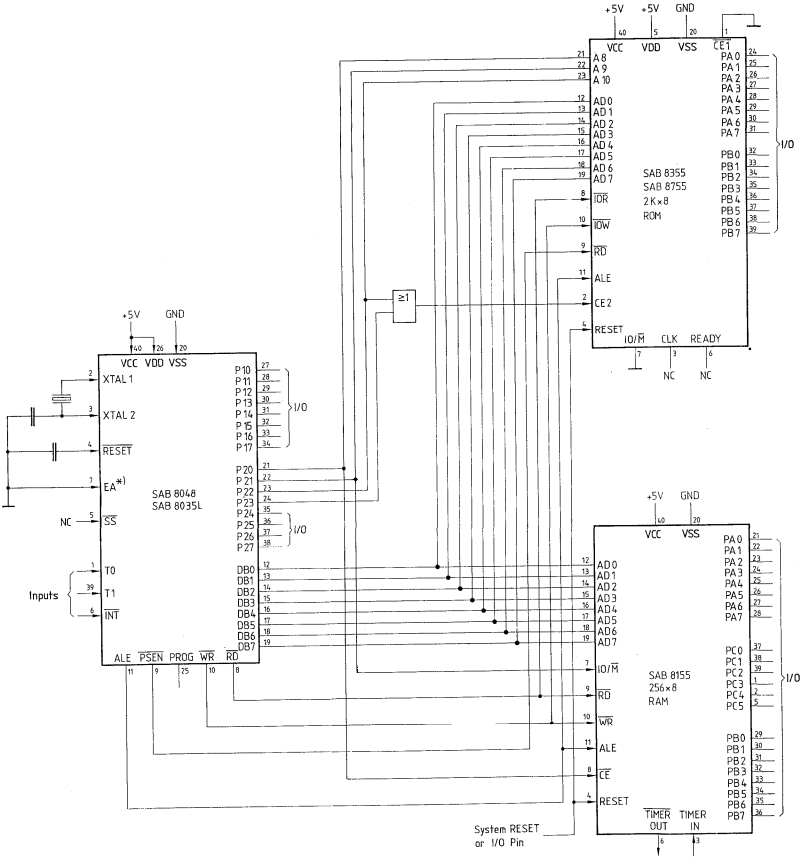


* EA = 5 V for SAB 8035L

Expansion of Program Memory and Data Memory

The application example shows the expansion of program memory, data memory, and I/O lines using the SAB 8355/8755 (2 K × 8 ROM, 16 I/O lines) and the SAB 8155 (256 × 8 RAM, 22 I/O lines, 14-bit timer).

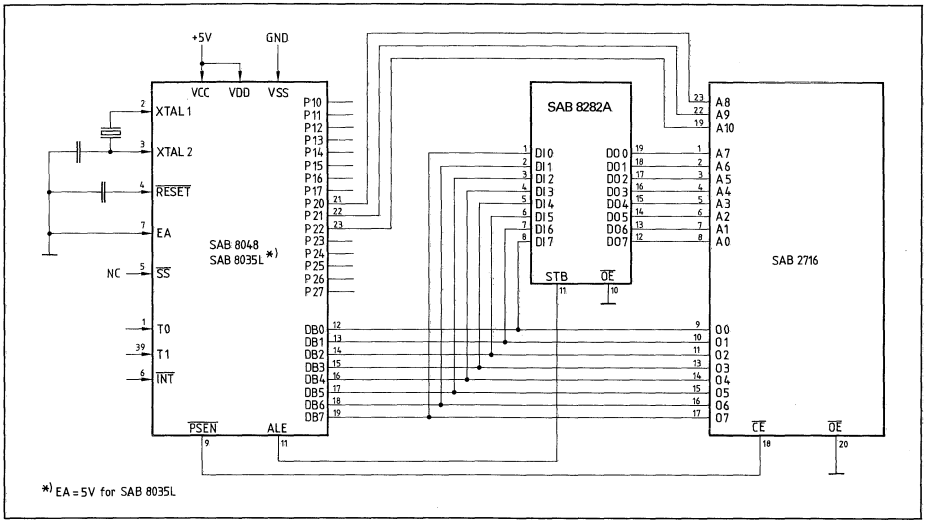
The SAB 8048 port I/O lines are reduced from 24 to 12 by adding 38 more I/O lines of the external devices.



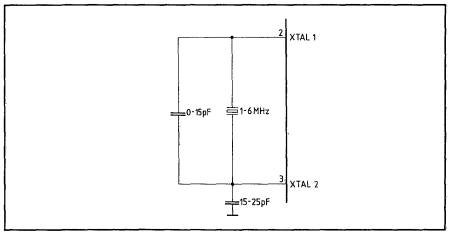
* EA = 5 V for SAB 8035L

Adding External Program Memory with EPROM SAB 2716

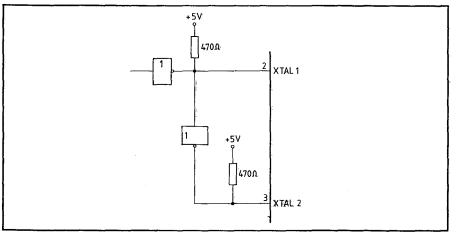
The SAB 8282A serves as a latch to separate addresses from the data bus



Connecting the Oscillator Inputs



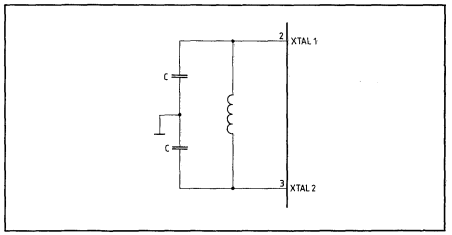
Crystal series resistance should be
$< 75\ \Omega$ at 6 MHz and $< 180\ \Omega$ at 3.6 MHz.



Both XTAL1 and XTAL2 should be driven.

Resistors to VCC are needed to ensure VIH = 3.8 V if TTL circuitry is used.

XTAL1 and XTAL2 must be high 35–65% of the period.

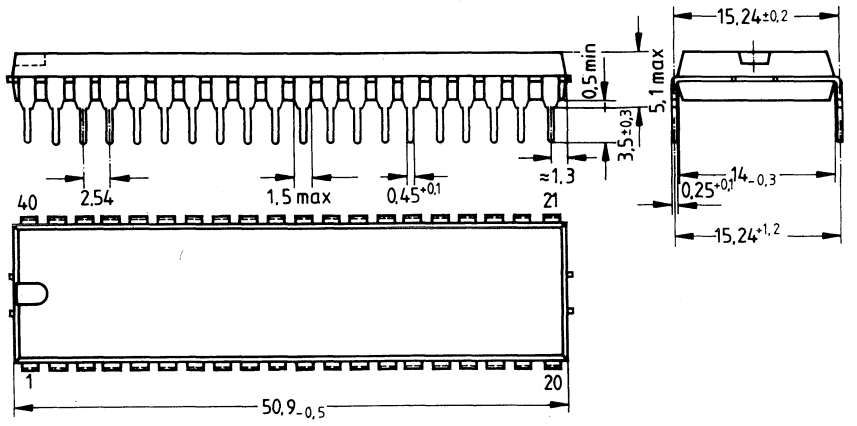


$$f = \frac{1}{2\pi\sqrt{LC'}} \qquad C' = \frac{C + 3\,CPP}{2}$$

CPP $\approx$ 5–10 pF pin-to-pin capacitance

Package Outline

Plastic Package, P-DIP, 40 pins



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 8048-P	Q67120-C32	8-bit single-chip microcomputer with maskprogrammable ROM (P-DIP)
SAB 8035L-P	Q67120-C43	with external ROM (P-DIP)

Preliminary

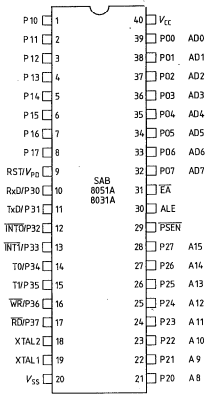
SAB 8051A/8031A
SAB 8051A-16/8031A-16
8-Bit Single-Chip Microcontroller

SAB 8051A/8051A-16 Microcontroller with factory-maskprogrammable ROM
SAB 8031A/8031A-16 Microcontroller for external ROM

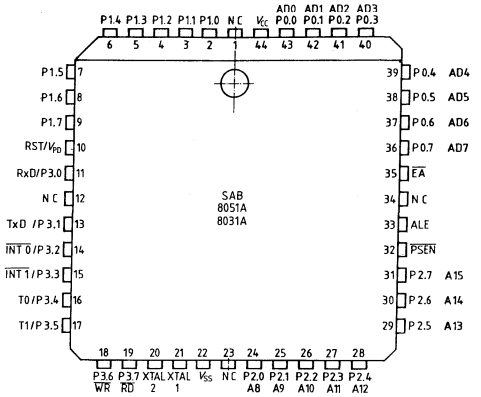
- SAB 8051A/8031A, 12 MHz operation
  SAB 8051A-16/8031A-16, 16 MHz operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128 Kbyte
- Compatible with SAB 8080/8085 peripherals
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in:
  1 µs (SAB 8051A/8031A)
  750 ns (SAB 8051A-16/8031A-16)
- 4 µs (3 µs) multiply and divide
- P-DIP-40 and PL-CC-44 package

Pin Configuration

P-DIP-40



PL-CC-44

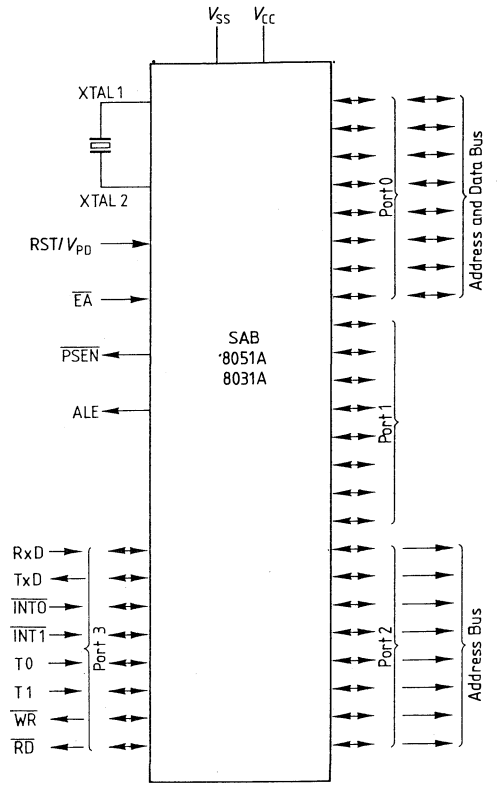


The SAB 8051A/8031A is a standalone, high-performance single-chip microcontroller fabricated in +5V advanced Siemens MYMOS (III) technology and supplied in a 40-pin plastic P-DIP or 44-pin plastic leaded chip carrier (PL-CC-44) package. It provides the hardware features, architectural enhancements and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data storage.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full-duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL-compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Logic Symbol



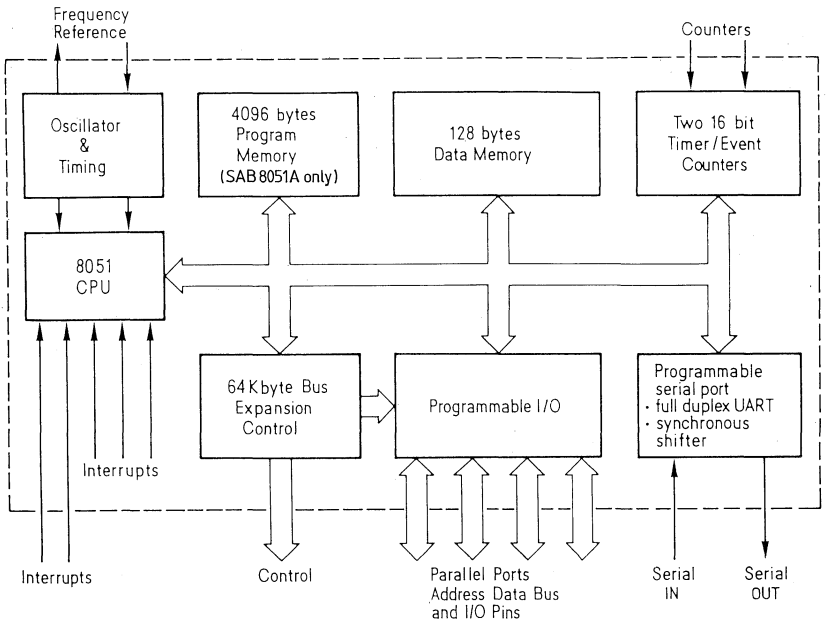
Pin Definitions and Functions

Symbol	Pin P-DIP-40	Pin PL-CC-44	Input (I) Output (O)	Function
P1.0–P1.7	1–8	2–9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20		XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	24–31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
$\overline{EA}$	31	35	I	When held at a TTL high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051A fetches all instructions from external program memory. For the SAB 8031A this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44		+5 V power supply during operation and program verification.
V_{SS}	20	22		Ground (0V)
NC	–	1, 12 23, 34	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/VPD and XTAL2)	2.0	V_{CC} +0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL2	2.5	V_{CC} +0.5	v	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = −80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = −400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	−500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	−3.2	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC}−1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 8031A/8051A SAB 8031A-16/8051A-16	– –	125 140	mA mA	All outputs disconnected
I_{PD}	Power down current	–	10	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

AC Characteristics for SAB 8051A/8031A

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2\,t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4\,t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3\,t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3\,t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5\,t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6\,t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6\,t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2\,t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5\,t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2\,t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8\,t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9\,t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3\,t_{CLCL}-50$	$3\,t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4\,t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7\,t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 8051A to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Clock Drive XTAL2

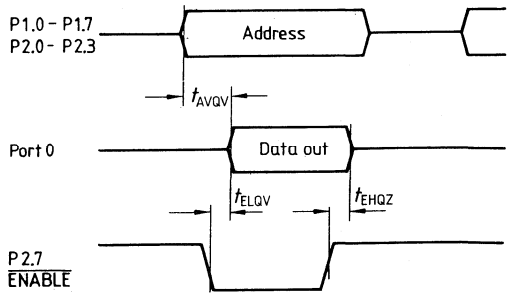
Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

ROM Verification Characteristics for SAB 8051A

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

Inputs: P2.4–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
$R_{ST}/V_{PD} = V_{IH1}$

AC Characteristics for SAB 8051A-16/8031A-16

T_A = 0 to 70°C; V_{CC} = 5V ±10%; V_{SS} = 0V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	85	–	$2\,t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	33	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	28	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4\,t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	153	–	$3\,t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	88	–	$3\,t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	48	–	$t_{CLCL}-15$	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	60	–	$t_{CLCL}-3$	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5\,t_{CLCL}-90$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	275	–	$6\,t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	$6\,t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2\,t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	148	–	$5\,t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	55	–	$2\,t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8\,t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9\,t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3\,t_{CLCL}-50$	$3\,t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4\,t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	288	–	$7\,t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 8051A-16 to devices with float times up to 55ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Clock Drive XTAL2

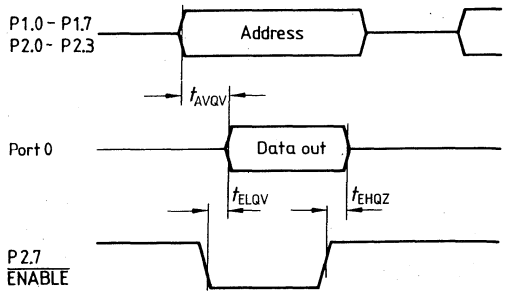
Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 16 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	62.5	833.3	ns
t_{CHCX}	High time	15	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	15	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	15	ns
t_{CHCL}	Fall time	–	15	ns

ROM Verification Characteristics for SAB 8051A-16

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

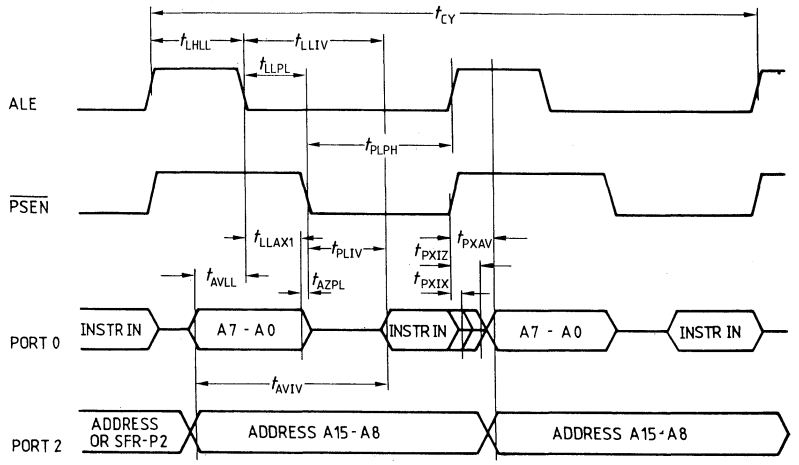


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

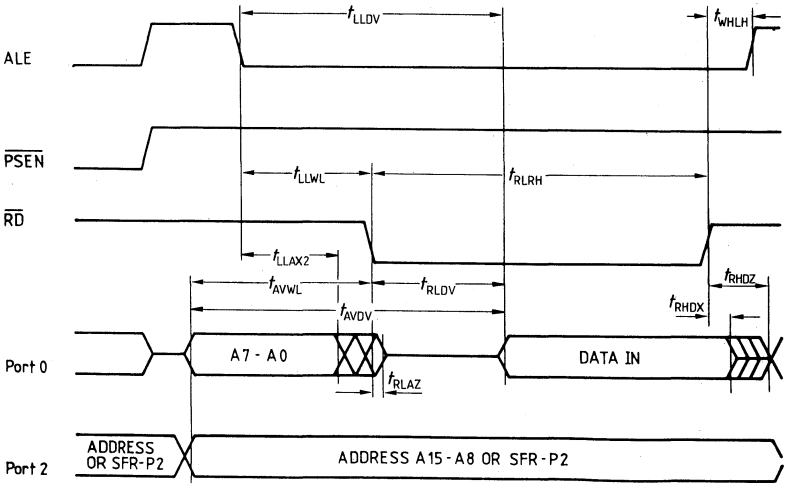
Inputs: P2.4–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
RST/$V_{PD} = V_{IH1}$

Waveforms

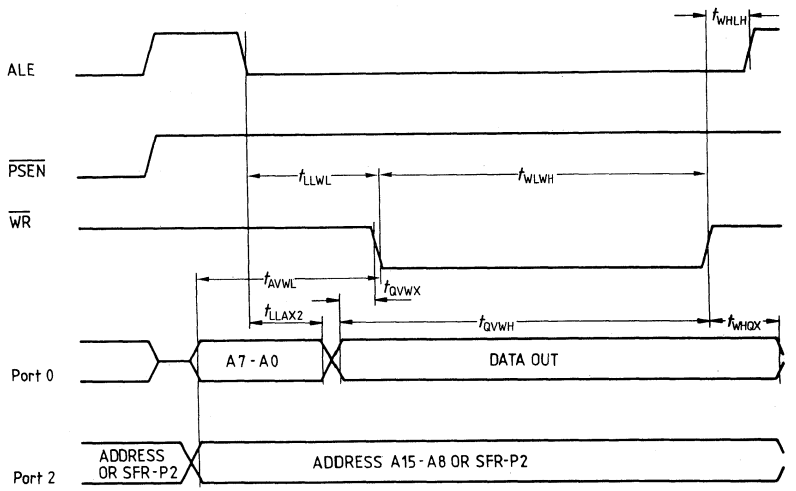
Program Memory Read Cycle



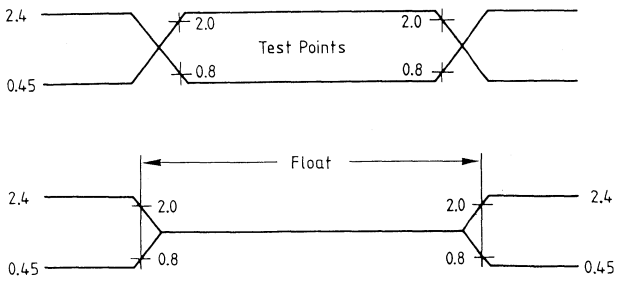
Data Memory Read Cycle



Data Memory Write Cycle

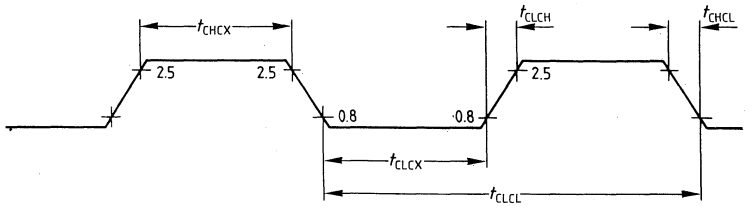


AC Testing Input, Output, Float Waveforms

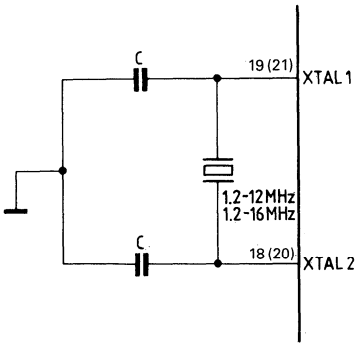


AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

External Clock Cycle

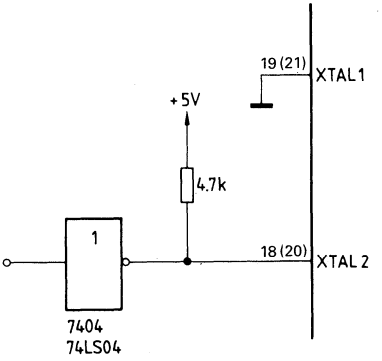


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

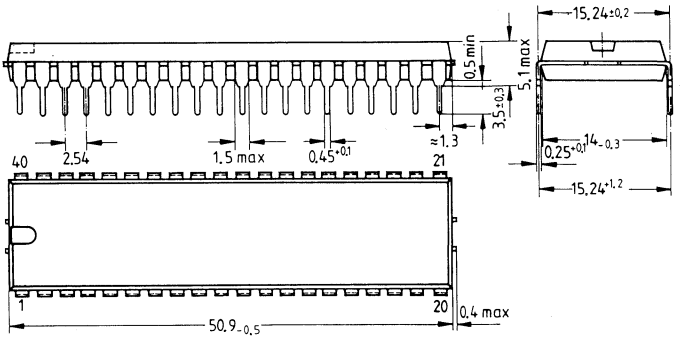
Crystal Oscillator Mode



Driving from External Source

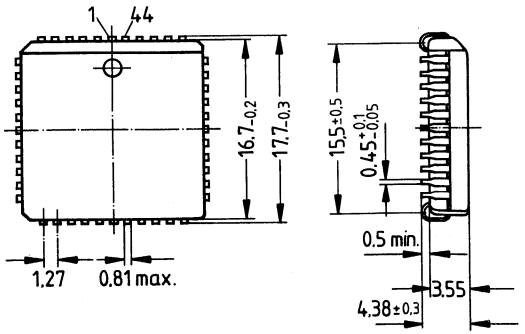
Pin number in (...) are for PL-CC-44 package

Plastic Package, P-DIP-40



Dimensions in mm

Plastic Package, PL-CC-44



Dimensions in mm

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcontroller
SAB 8051A-P	Q 67120-C186	with mask-programmable ROM (P-DIP-40)
SAB 8031A-P	Q 67120-C183	for external memory (P-DIP-40)
SAB 8051A-16-P	Q 67120-C346	with mask-programmable ROM (P-DIP-40)
SAB 8031A-16-P	Q 67120-C347	for external memory (P-DIP- 40)
SAB 8051A-N	Q 67120-C224	with mask-programmable ROM (PL-CC-44)
SAB 8031A-N	Q 67120-C271	for external memory (PL-CC-44)
SAB 8051A-16-N	Q 67120-C348	with mask-programmable ROM (PL-CC-44)
SAB 8031A-16-N	Q 67120-C349	for external memory (PL-CC-44)

Advance Information

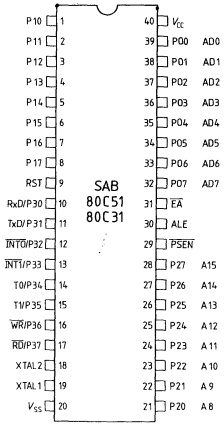
SAB 80C51/80C31
8-Bit CMOS Microcontroller

SAB 80C51-P(N) CMOS microcontroller with factory mask-programmable ROM
SAB 80C31-P(N) CMOS microcontroller for external ROM

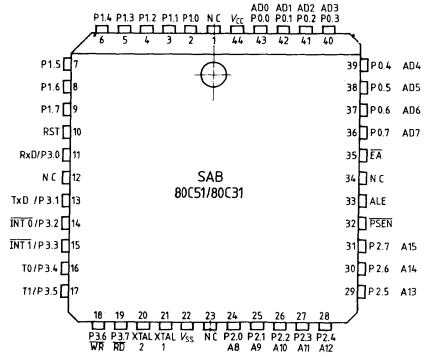
- 4K × 8 ROM (SAB 80C51 only)
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable up to 128 Kbytes
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- 5 interrupt sources, two priority levels
- Idle and power-down operation
- P-DIP 40 and PLCC 44 package

Pin Configuration

P-DIP-40



PL-CC-44



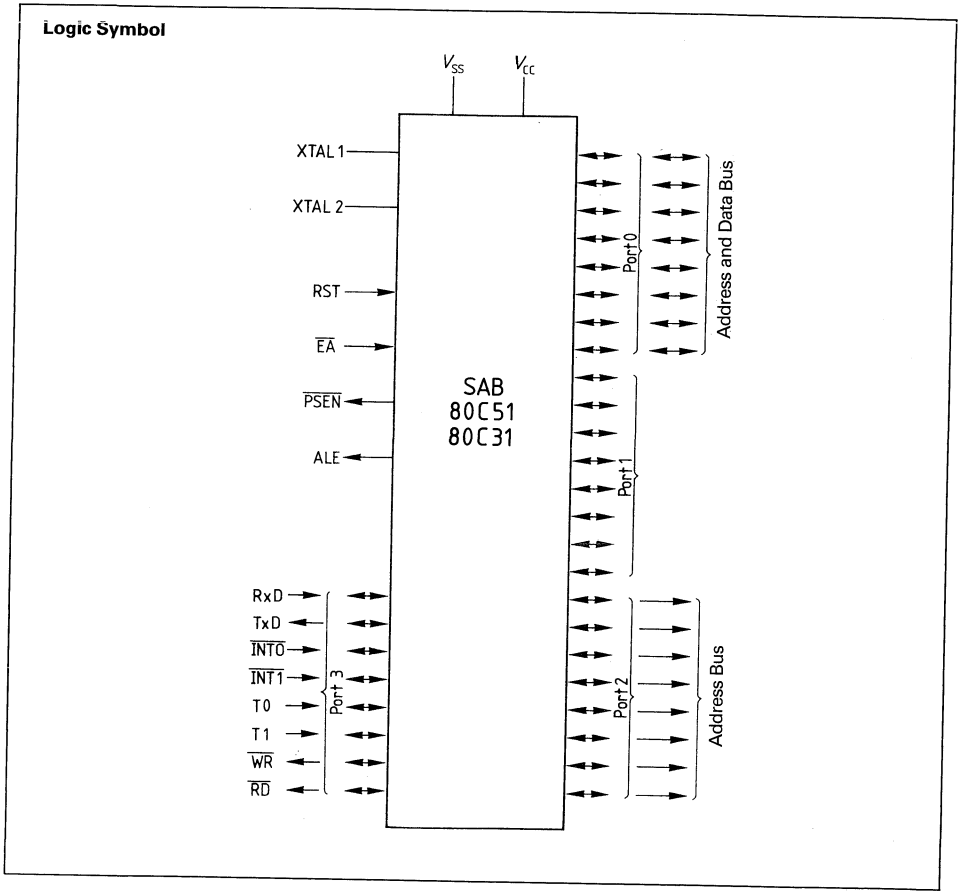
The SAB 80C51/80C31 is a standalone, high-performance CMOS single-chip microcontroller, designed in Siemens ACMOS technology. It is functionally compatible with the SAB 8051A/8031A devices in MYMOS technology.

The low-power properties of ACMOS technology allow applications where power consumption and dissipation are critical. In addition, the SAB 80C51/80C31 has two software-selectable modes of reduced activity for further power reduction – idle and power-down.

The SAB 80C51 contains a non-volatile 4K × 8 read-only program memory, a volatile 128 × 8 read/write data memory, 32 I/O lines, two 16-bit timer/counters, a five-source, two-priority-level interrupt structure, a serial I/O port, an on-chip oscillator, and clock circuits. The SAB 80C31 is identical, except that it lacks the program memory on the chip.

The SAB 80C51/80C31 is supplied in a 40-pin plastic dual-in-line (P-DIP-40) package or a 44-pin plastic leaded chip carrier (PL-CC-44) package.

Logic Symbol



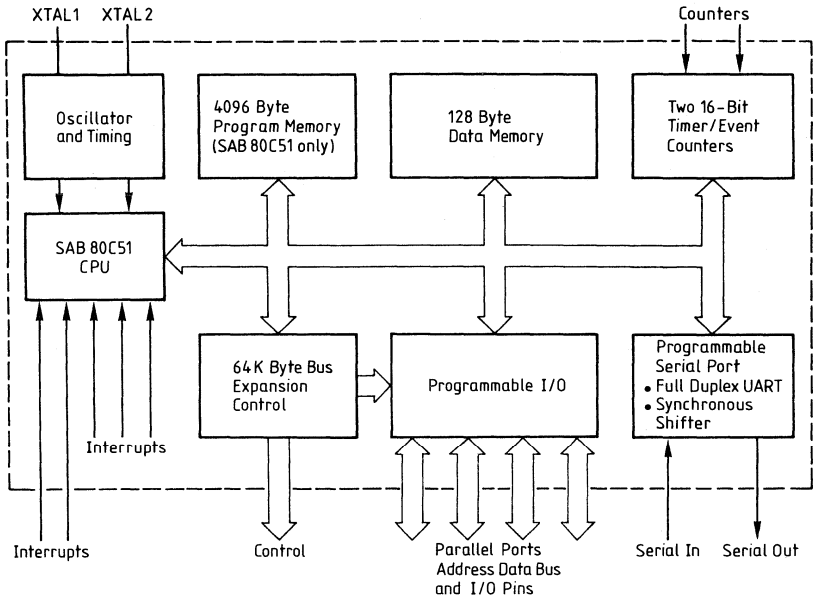
Pin Definitions and Functions

Symbol	Pin P-DIP-40	Pin PL-CC-44	Input (I) Output (O)	Functions
P1.0–P1.7	1–8	2–9	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 1 also receives the low-order address bytes during program verification.
RST	9	10	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20		**XTAL 1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL2** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL 2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-DIP-40	Pin PL-CC-44	Input (I) Output (O)	Functions
P2.0–P2.7	21–28	24–31	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	29	32	O	**$\overline{\text{PROGRAM STORE ENABLE}}$** This output issues a control signal that enables the external program memory to access the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	**ADDRESS LATCH ENABLE** Provides signal used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	31	35	I	**$\overline{\text{EXTERNAL ACCESS}}$** When held at a high level, the SAB 80C51 executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 80C51 fetches all instructions from the external program memory. For the SAB 80C31 this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C51. External pullup resistors are required during program verification.
V_{CC}	40	44		**Supply Voltage** during normal, idle, and power-down operations.
V_{SS}	20	22		**Circuit Ground Potential**
N.C.	–	1, 12, 23, 34	–	**No connection**

Block Diagram



Functional Description

The SAB 80C51/80C31 is functionally compatible with the SAB 8051A/8031A products that are designed in Siemens MYMOS technology.

In addition, instead of the RAM backup power supply of the SAB 8051A/8031A, the SAB 80C51/80C31 offers two additional power control modes, the idle mode and the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

- Idle mode
  In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction that invokes the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The contents of the CPU, the on-chip RAM, and all the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor in the same way as a power-on reset.
- Power-down mode
  In the power-down mode the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. Only the contents of the on-chip RAM is preserved. A hardware reset is the only way to terminate power-down.

During power-down and idle mode the external pins will have the following status (see table 1):

Table 1
Status of the External Pins during Idle and Power-Down Modes

Mode	Program Memory	ALE	PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data	Data	Data/ Alternate Outputs
Idle	External	1	1	Float	Data	Address	Data/ Alternate Outputs
Power-Down	Internal	0	0	Data	Data	Data	Data/Last Output of Alternate Function
Power-Down	External	0	0	Float	Data	Data	Data/Last Output of Alternate Function

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn — Working register R0–R7
direct — 128 internal RAM locations, any I/O port, control or status register
@Ri — Indirect internal or external RAM location addressed by register R0 or R1
#data — 8-bit constant included in instruction
#data 16 — 16-bit constant included as bytes 2 and 3 of instruction
bit — 128 software flags, any I/O pin, control or status bit
A — Accumulator

Notes on program addressing modes:

addr 16 — Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 — Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex code	Number of bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A, ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 V to V_{CC} +0.5 V
Voltage on V_{CC} to V_{SS}	−0.5 to 6.5 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 20%; V_{SS} = 0 V; T_A = 0 to 70°C

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage (except EA)	V_{IL}	−0.5	$0.2V_{CC}-0.1$	V	–
Input low voltage (EA)	V_{IL1}	−0.5	$0.2V_{CC}-0.3$	V	–
Input high voltage (except XTAL1, RST)	V_{IH}	$0.2V_{CC}+0.9$	$V_{CC}+0.5$	V	–
Input high voltage (XTAL1, RST)	V_{IH1}	$0.7V_{CC}$	$V_{CC}+0.5$	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, PSEN)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4	–	V	I_{OH} = −60 µA V_{CC} = 5V ±10%
		$0.9V_{CC}$	–	V	I_{OH} = −10 µA
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4	–	V	I_{OH} = −400 µA V_{CC} = 5V ±10%
		$0.9V_{CC}$	–	V	I_{OH} = −40 µA [2]
Logical 0 input current (ports 1, 2, 3)	I_{IL}	–	−50	µA	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	–	−650	µA	V_{IN} = 2V
Input leakage current (port 0, EA)	I_{LI}	–	±10	µA	$0.45 < V_{IN} < V_{CC}$
Reset pulldown resistor	R_{RST}	50	150	kΩ	–
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25°C
Power down current	I_{PD}	–	50	µA	V_{CC} = 2 to 6V [3]

For notes refer to next page.

DC Characteristics (cont'd)

Maximum I_{CC} (mA)

		Active Mode [4]			Idle Mode [5]		
Freq.	V_{CC}	4 V	5 V	6 V	4 V	5 V	6 V
0.5 MHz		1.6	2.2	3	0.6	0.9	1.2
3.5 MHz		4.3	5.7	7.5	1.1	1.6	2.2
8.0 MHz		8.3	11	14	1.8	2.7	3.7
12 MHz		12	16	20	2.5	3.7	5

Note [1]: Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading >100pF), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

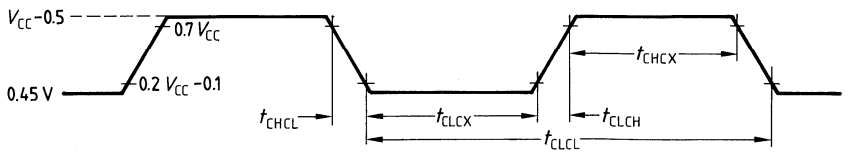
Note [2]: Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

Note [3]: Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = V_{CC}; XTAL1 = V_{SS}; XTAL2 = N.C.; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

Note [4]: I_{CC} (active mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = Port 0 = V_{CC}; $\overline{RESET}$ = V_{CC}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

Note [5]: I_{CC} (idle mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = V_{CC}; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode
$t_{CLCH} = t_{CHCL}$ = 5 ns



AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±20%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}$-40	–	ns
Address setup to ALE	t_{AVLL}	28	–	t_{CLCL}-55	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL}-35	–	ns
ALE to valid instruction in	t_{LLIV}	–	234	–	$4t_{CLCL}$-100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	43	–	t_{CLCL}-40	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	205	–	$3t_{CLCL}$-45	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	145	–	$3t_{CLCL}$-105	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	59	–	t_{CLCL}-25	ns
Address to valid instruction in	t_{AVIV}	–	312	–	$5t_{CLCL}$-105	ns
$\overline{PSEN}$ to address float	t_{PLAZ}	–	10	–	10	ns

External Data Memory Characteristics

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL}$-100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL}$-100	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL}-35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL}$-165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL}$-70	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL}$-150	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL}$-165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	$4t_{CLCL}$-130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	23	–	t_{CLCL}-60	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL}-50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

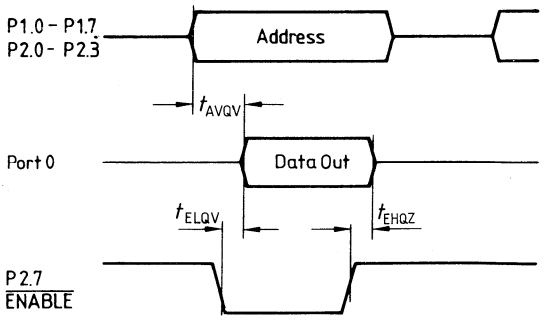
Parameter	Symbol	Limit values		Unit
		Variable clock Freq. = 0.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	2000	ns
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	12	MHz

ROM Verification Characteristics for SAB 80C51

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\,V \pm 20\%$; $V_{SS} = 0\,V$

Parameter	Symbol	Limit values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
$\overline{\text{ENABLE}}$ to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after $\overline{\text{ENABLE}}$	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification

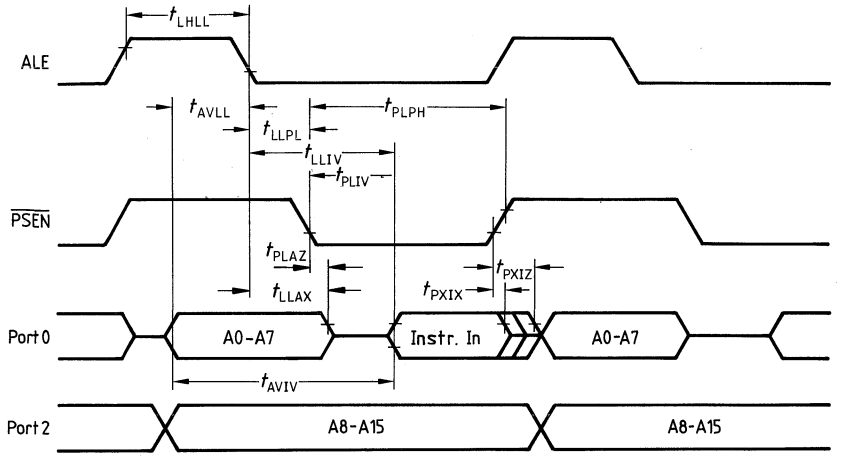


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

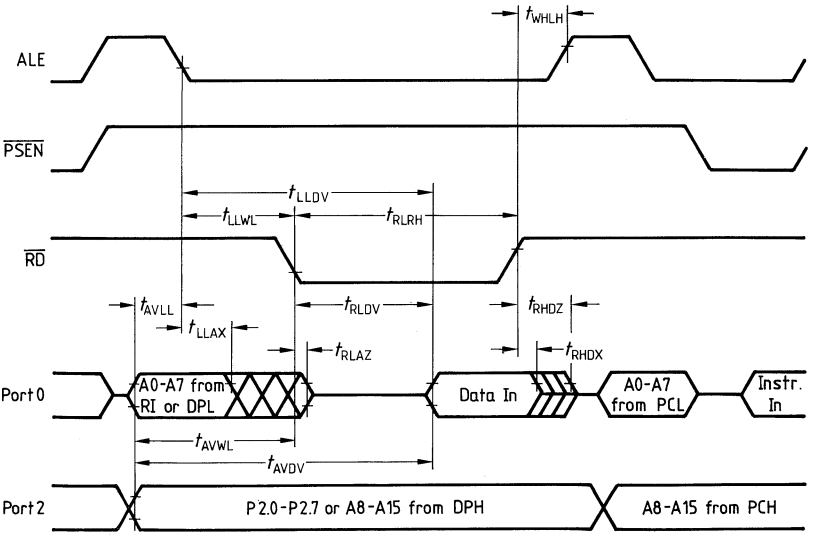
Inputs: P2.4–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
RST $= V_{IH1}$

Waveforms

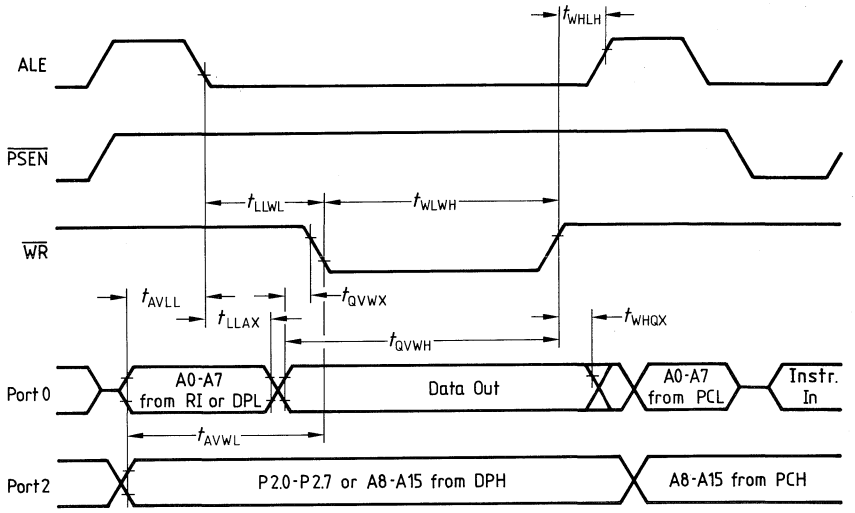
Program Memory Read Cycle



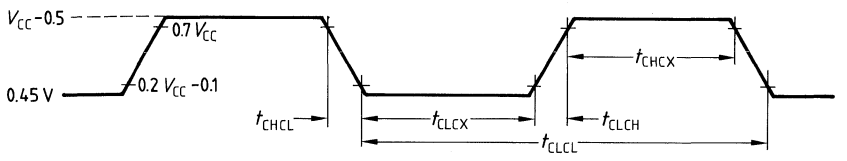
Data Memory Read Cycle



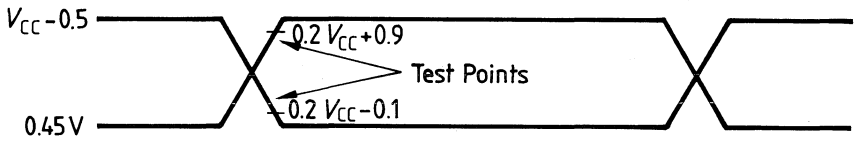
Data Memory Write Cycle



External Clock Cycle

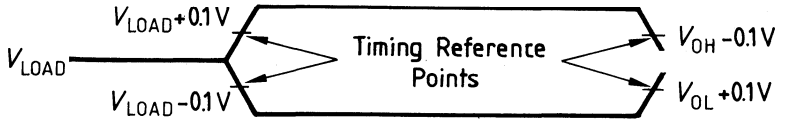


AC Testing: Input, Output Waveforms



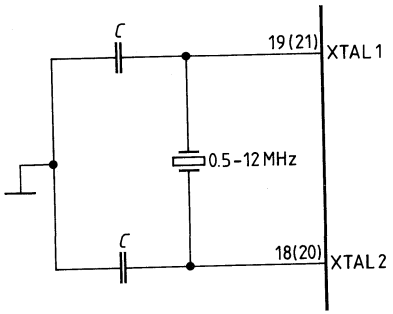
AC Inputs during testing are driven at $V_{CC}-0.5V$ for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at $V_{IH\,min}$ for a logic '1' and $V_{IL\,max}$ for a logic '0'.

AC Testing: Float Waveforms



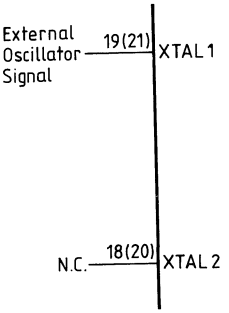
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

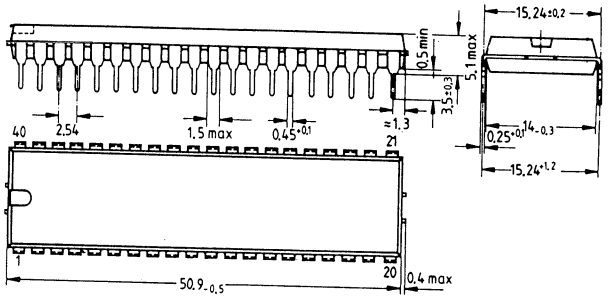
Crystal Oscillator Mode



Driving from External Source

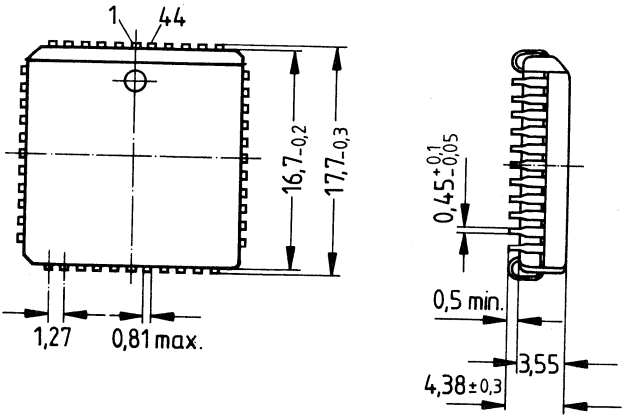
Pin numbers in (...) are for PLCC 44 package

Plastic Package, P-DIP-40



Dimensions in mm

Plastic Package, PLCC-44



Dimensions in mm

Ordering Information

Type	Ordering code	Description
		8-bit CMOS microcontroller
SAB 80C51-P	Q 67120-C265	with mask-programmable ROM (P-DIP-40)
SAB 80C31-P	Q 67120-C157	for external memory (P-DIP-40)
SAB 80C51-N	Q67120-C372	with mask-programmable ROM (PL-CC-44)
SAB 80C31-N	Q67120-C371	for external memory (PL-CC-44)

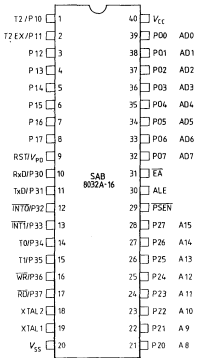
Preliminary

SAB 8032A-16
8-Bit Single Chip Microcontroller

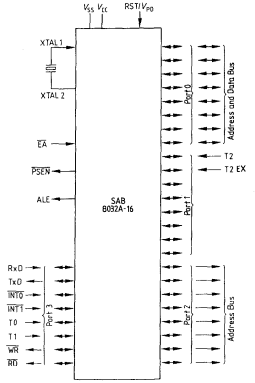
SAB 8032A-16 Control-oriented CPU with RAM and I/O, for external ROM

- 16 MHz operation
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128 Kbytes
- Compatible with SAB 8080/8085 peripherals
- Timer 2 capture capability
- Variable transmit/receive baud rate capability
- Boolean processor
- Most instructions execute in 750 ns
- 3 µs multiply and divide
- Upward compatible with SAB 8031A/8051A

Pin Configuration



Logic Symbol



The SAB 8032A is a stand-alone, high-performance single-chip microcomputer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin DIP.
It is upward compatible with the SAB 8031A/8051A. It provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The SAB 8032A-16 contains a volatile 256 × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level, nested interrupt structure, a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART, as well as an on-chip oscillator and clock circuits. The SAB 8032A-16 has to be operated with external program memory.

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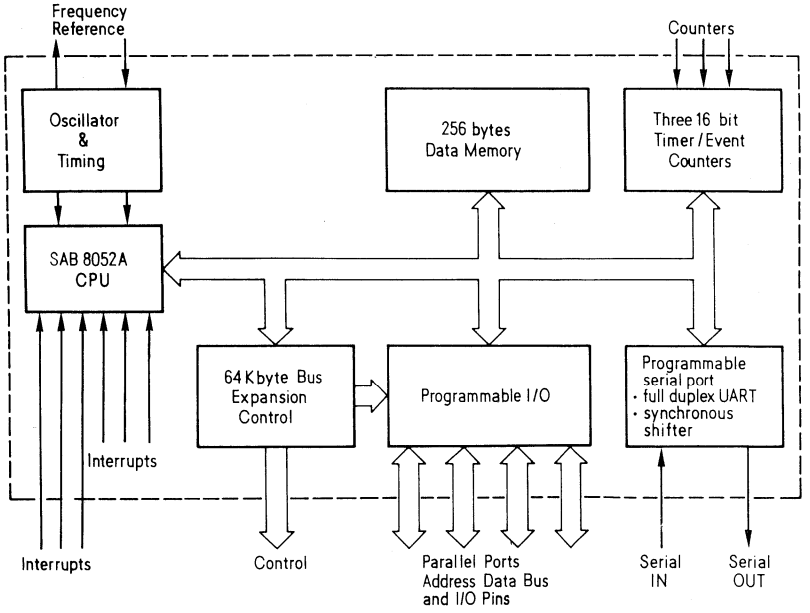
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
P1.0–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to Timer 2, and T2EX, Timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/VPD	9	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18		XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Number	Input (I) Output (O)	Function
ALE	30	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	I	For the SAB 8032A-16 this pin must be tied low.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40		+5V power supply during operation and program verification.
V_{SS}	20		Circuit ground potential.

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#*data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings[1)]

Ambient Temperature under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (V_{SS})	−0.5 to + 7 V
Power Dissipation	2 W

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage (Except RST/VPD and XTAL2)	2.0	V_{CC}+0.5		
V_{IH1}	Input High Voltage to RST/VPD for Reset, XTAL2	2.5			XTAL1 to V_{SS}
V_{PD}	Power Down Voltage to RST/VPD	4.5	5.5		V_{CC} = 0V
V_{OL}	Output Low Voltage Ports 1, 2, 3	–	0.45		I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage Port 0, ALE, $\overline{PSEN}$				I_{OL} = 3.2 mA
V_{OH}	Output High Voltage Ports 1, 2, 3	2.4	–		I_{OH} = −80 µA
V_{OH1}	Output High Voltage Port 0, ALE, $\overline{PSEN}$				I_{OH} = −400 µA
I_{IL}	Logical 0 Input Current Ports 1, 2, 3	–	−500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 Input Current XTAL 2		−2.0	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input High Current to RST/VPD for Reset		500	µA	V_{IN} = V_{CC} − 1.5 V
I_{LI}	Input Leakage Current to Port 0, $\overline{EA}$		± 10		0V < V_{IN} < V_{CC}
I_{CC}	Power Supply Current		175	mA	All outputs disconnected
I_{PD}	Power Down Current		15		V_{CC} = 0V
C_{IO}	Capacitance of I/O Buffer		10	pF	f_c = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

T_A = 0°C to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE Pulse Width	85	–	$2t_{CLCL}$-40	–	ns
t_{AVLL}	Address Setup to ALE	33	–	t_{CLCL}-30	–	
t_{LLAX1}	Address Hold after ALE	28	–	t_{CLCL}-35	–	
t_{LLIV}	ALE to Valid Instr In	–	150	–	$4t_{CLCL}$-100	
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	t_{CLCL}-25	–	
t_{PLPH}	$\overline{PSEN}$ Pulse Width	153	–	$3t_{CLCL}$-35	–	
t_{PLIV}	$\overline{PSEN}$ to Valid Instr In	–	88	–	$3t_{CLCL}$-100	
t_{PXIX}	Input Instr Hold after $\overline{PSEN}$	0	–	0	–	
$t_{PXIZ*)}$	Input Instr Float after $\overline{PSEN}$	–	48	–	t_{CLCL}-15	
$t_{PXAV*)}$	Address Valid after $\overline{PSEN}$	60	–	t_{CLCL}-3	–	
t_{AVIV}	Address to Valid Instr In	–	223	–	$5t_{CLCL}$-90	
t_{AZPL}	Address Float to $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

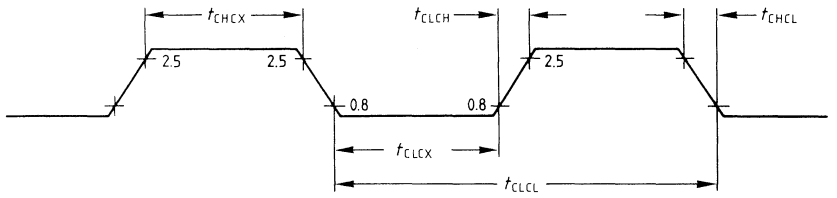
Symbol	Parameter	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ Pulse Width	275	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ Pulse Width	275	–	$6t_{CLCL}$-100	–	
t_{LLAX2}	Address Hold after ALE	90	–	$2t_{CLCL}$-35	–	
t_{RLDV}	$\overline{RD}$ to Valid Data In	–	148	–	$5t_{CLCL}$-165	
t_{RHDX}	Data Hold after $\overline{RD}$	0	–	0	–	
t_{RHDZ}	Data Float after $\overline{RD}$	–	55	–	$2t_{CLCL}$-70	
t_{LLDV}	ALE to Valid Data In	–	350	–	$8t_{CLCL}$-150	
t_{AVDV}	Address to Valid Data In	–	398	–	$9t_{CLCL}$-165	
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3t_{CLCL}$-50	$3t_{CLCL}$+50	
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4t_{CLCL}$-130	–	
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	23	103	t_{CLCL}-40	t_{CLCL}+40	
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	13	–	t_{CLCL}-50	–	
t_{QVWH}	Data Setup before $\overline{WR}$	288	–	$7t_{CLCL}$-150	–	
t_{WHQX}	Data Hold after $\overline{WR}$	13	–	t_{CLCL}-50	–	
t_{RLAZ}	Address Float after $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8032A-16 to devices with float times up to 55ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

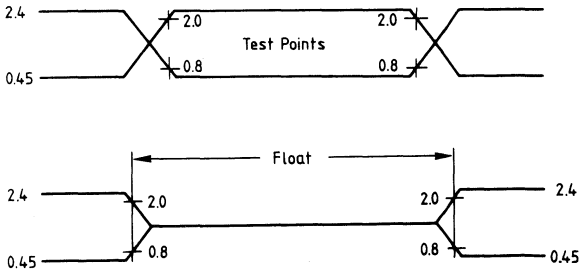
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 16 MHz		
		min.	max.	
t_{CLCL}	Oscillator Period	62.5	833.3	ns
t_{CHCX}	High Time	15	t_{CLCL}-t_{CLCX}	
t_{CLCX}	Low Time	15	t_{CLCL}-t_{CHCX}	
t_{CLCH}	Rise Time	–	15	
t_{CHCL}	Fall Time	–	15	

External Clock Cycle



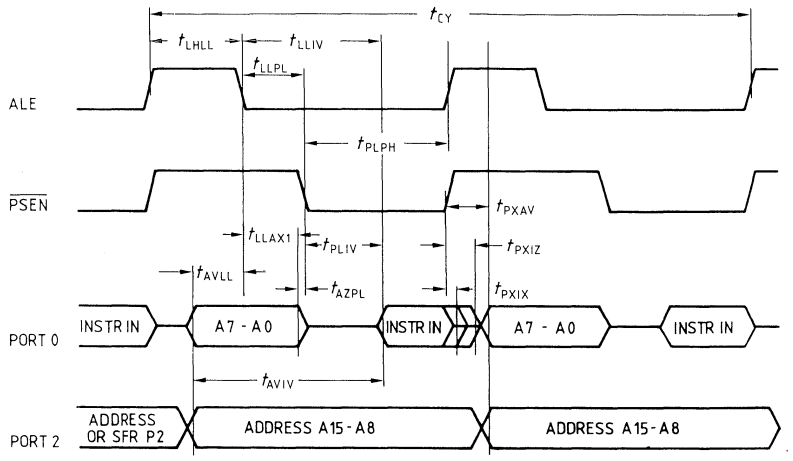
A.C. Testing Input, Output, Float Waveforms



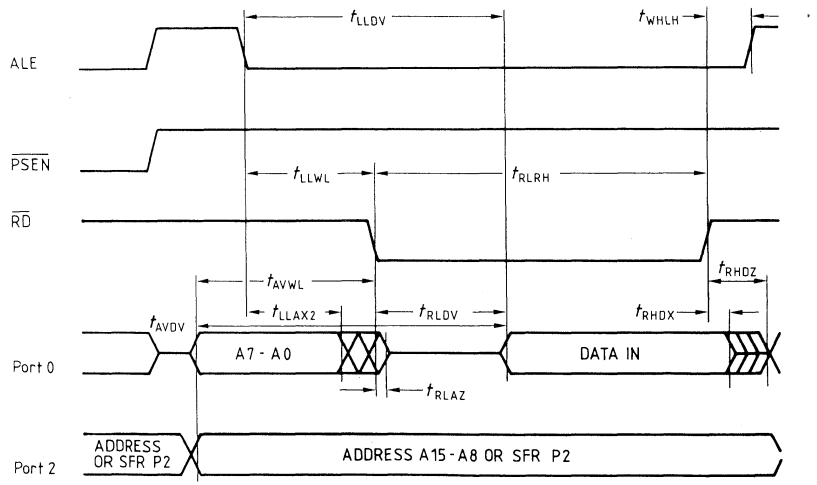
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

Waveforms

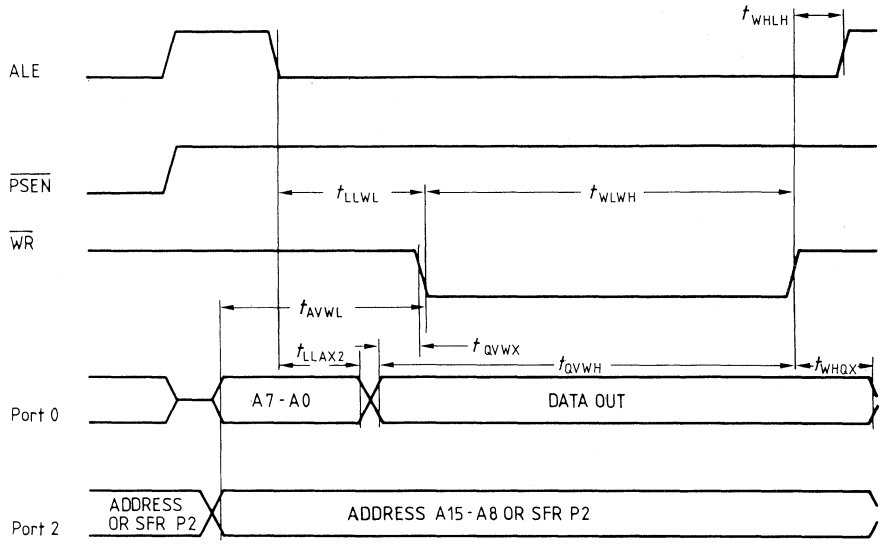
Program Memory Read Cycle



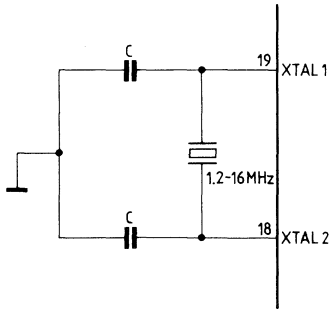
Data Memory Read Cycle



Data Memory Write Cycle

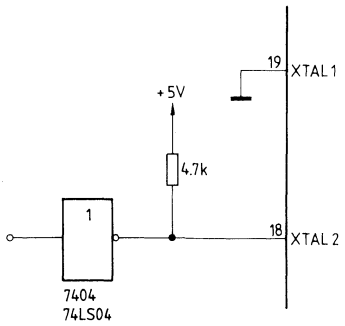


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

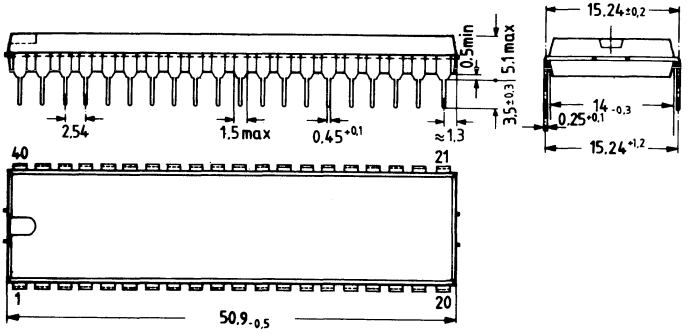
Crystal Oscillator Mode



Driving from External Source

Package Outlines

Plastic Package, P-DIP, 40 Pins



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 8032A-16-P	Q 67120-C350	8-Bit Single-Chip Microcontroller for External Memory (P-DIP)

Preliminary

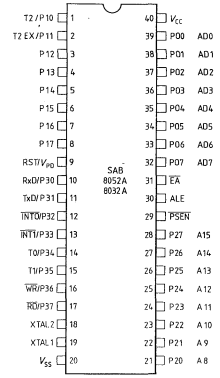
SAB 8052A/8032A
8-Bit Single-Chip Microcontroller

SAB 8052A-P(N) Microcontroller with factory-maskprogrammable ROM
SAB 8032A-P(N) Microcontroller for external ROM

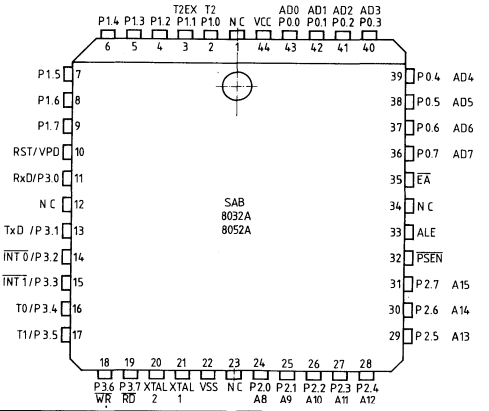
- 8K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- P-DIP40 and PLCC44 package
- Full backward compatibility with SAB 8051/8031

Pin Configuration

P-DIP 40



PLCC 44

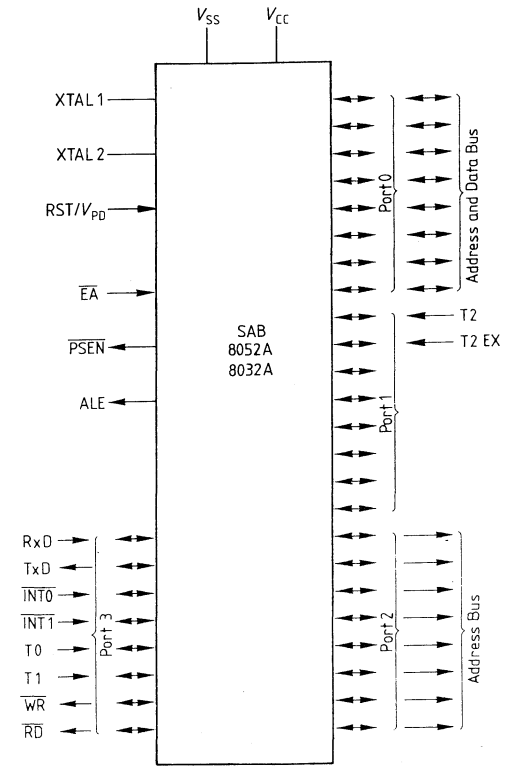


The SAB 8052A/8032A is a standalone, high-performance single-chip microcontroller fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin DIP or 44-pin plastic leaded chip carrier (PLCC44) package. It is backwardly compatible with the SAB 8051A/8031A. It provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The SAB 8052A contains a non-volatile 8 K × 8 read-only program memory; a volatile 256 × 8 read/write data memory; 32 I/O lines; three 16-bit timer/counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical with the SAB 8052A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8052A can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Logic Symbol



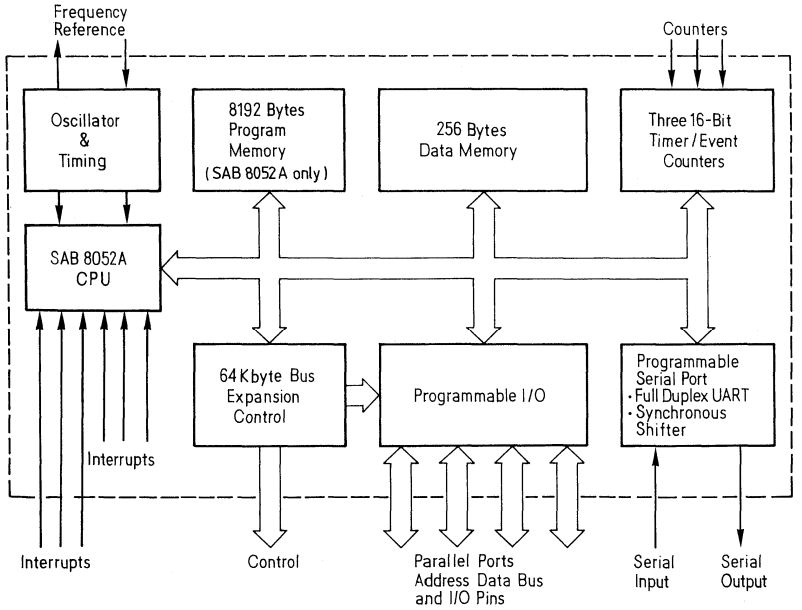
Pin Definitions and Functions

Symbol	Pin DIP40	Pin PLCC44	Input (I) Output (O)	Function
P1.0–P1.7	1–8	2–9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19, 18	21, 20	I	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	24–31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin DIP40	Pin PLCC44	Input (I) Output (O)	Function
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+5V power supply during operation and program verification.
V_{SS}	20	22	–	Circuit ground potential.
NC	–	1, 12, 23, 24	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#*data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to +7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL2)	2.0	V_{CC}+0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL2	2.5	V_{CC}+0.5	V	XTAL1 to V_{SS}
V_{PD}	Power-down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = −80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = −400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	−500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	−2.0	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC}−1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	0V < V_{IN} < V_{CC}
I_{CC}	Power supply current	–	175	mA	All outputs disconnected
I_{PD}	Power-down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics

T_A = 0°C to 70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} [1]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} [1]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

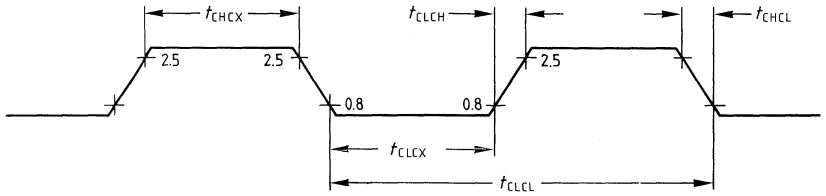
[1] Interfacing the SAB 8052A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Clock Drive XTAL2

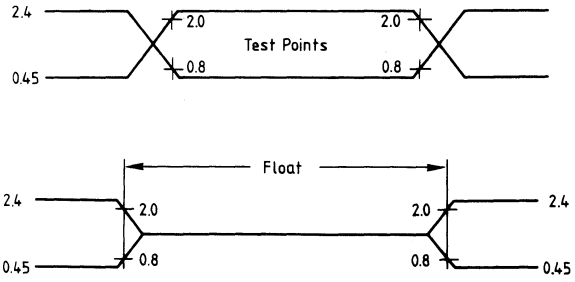
Symbol	Parameter	Limit values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

Waveforms

External Clock Cycle

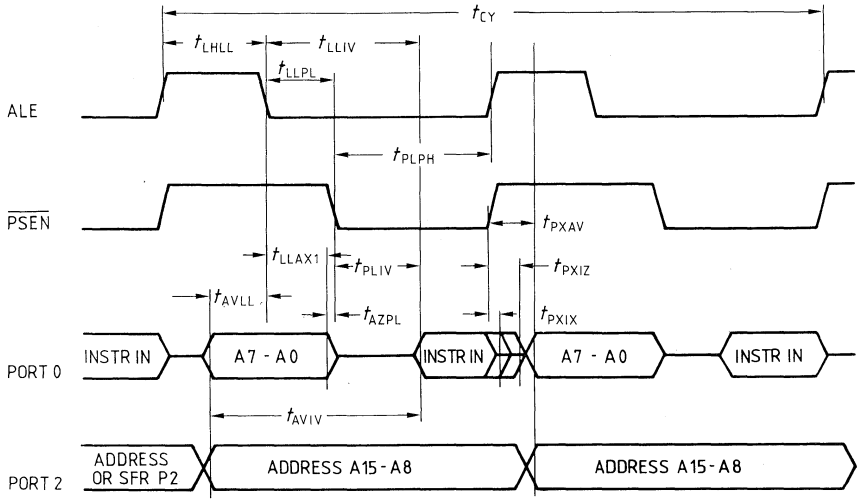


AC Testing Input, Output, Float Waveforms

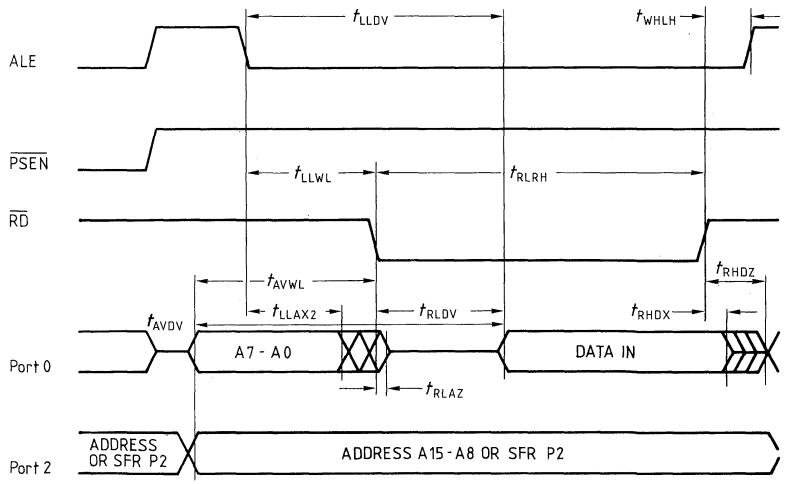


AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

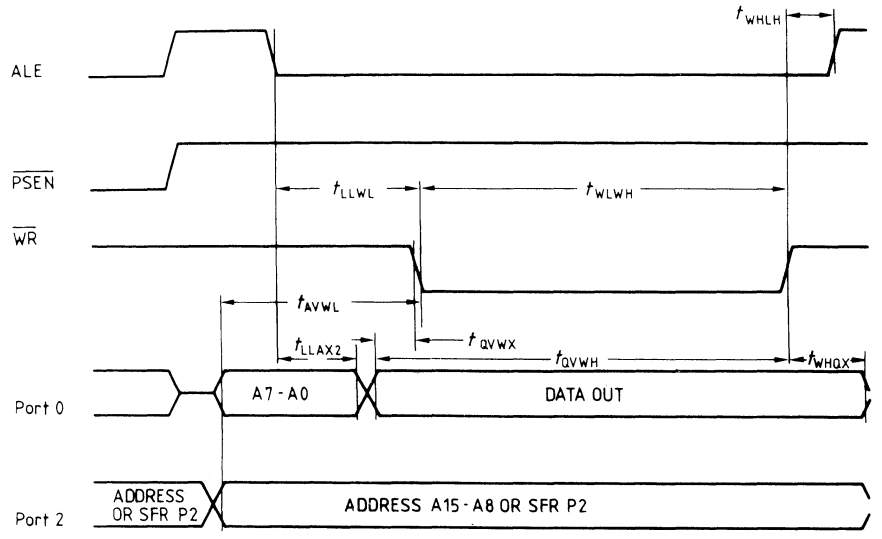
Program Memory Read Cycle



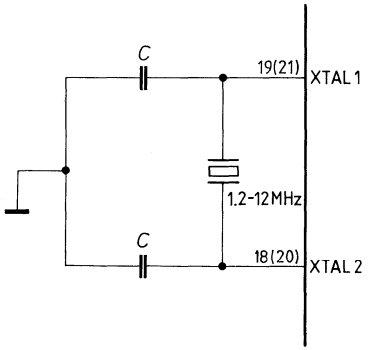
Data Memory Read Cycle



Data Memory Write Cycle

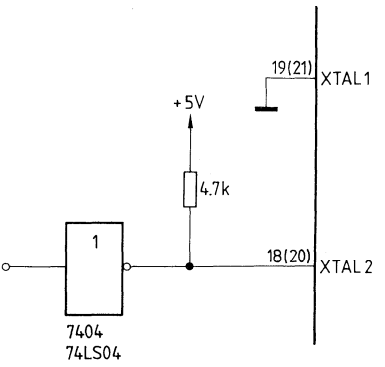


Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode



Driving from External Source

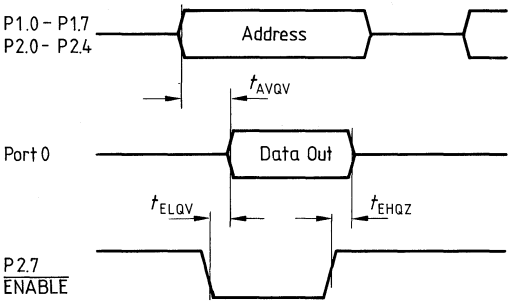
Pin numbers in (...) are specified for PLCC44 package.

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	$48\,t_{CLCL}$	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	$48\,t_{CLCL}$	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	$48\,t_{CLCL}$	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



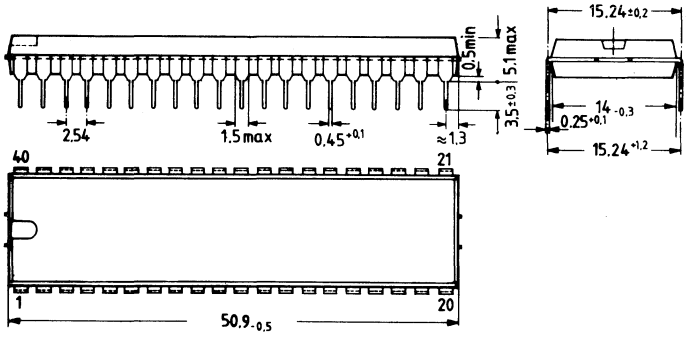
Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

Inputs: P2.5–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}}$ = TTL high level
RST/V_{PD} = V_{IH1}

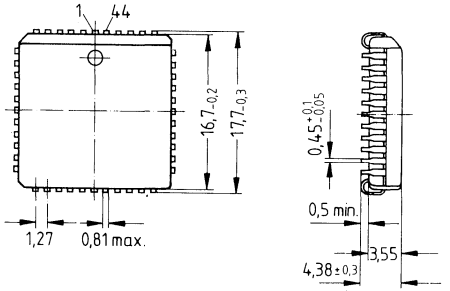
Package Outlines

Plastic Package, P-DIP, 40 Pins



Dimensions in mm

Plastic Package, PLCC, 44 Pins



Dimensions in mm

Ordering Information

Type	Description	Ordering code
	8-bit single-chip microcontroller	
SAB 8052A-P	with mask-programmable ROM (P-DIP40)	Q 67120-C195
SAB 8032A-P	for external memory (P-DIP40)	Q 67120-C196
SAB 8052A-N	with mask-programmable ROM (PLCC44)	Q 67120-C263
SAB 8032A-N	for external memory (PLCC44)	Q 67120-C264

Advance Information

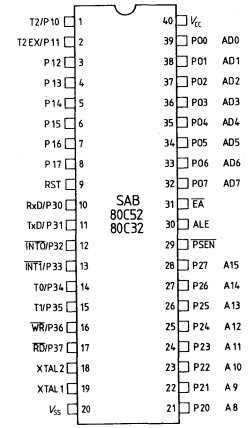
SAB 80C52/80C32
8-Bit CMOS Microcontroller

SAB 80C52-P(N) CMOS microcontroller with factory-maskprogrammable ROM
SAB 80C32-P(N) CMOS microcontroller for external ROM

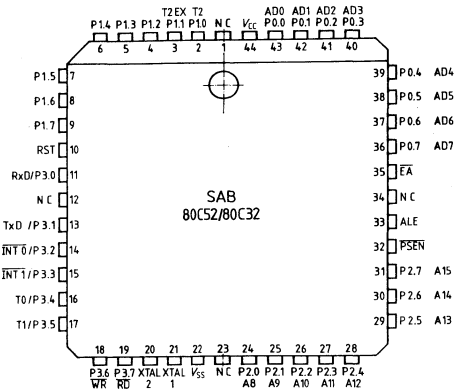
- 8K × 8 ROM (SAB 80C52 only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- Six interrupt sources, two priority levels
- Idle and power-down operation
- P-DIP 40 and PLCC 44 package
- Full backward compatibility with SAB 80C51/80C31

Pin Configuration

P-DIP-40



PL-CC-44



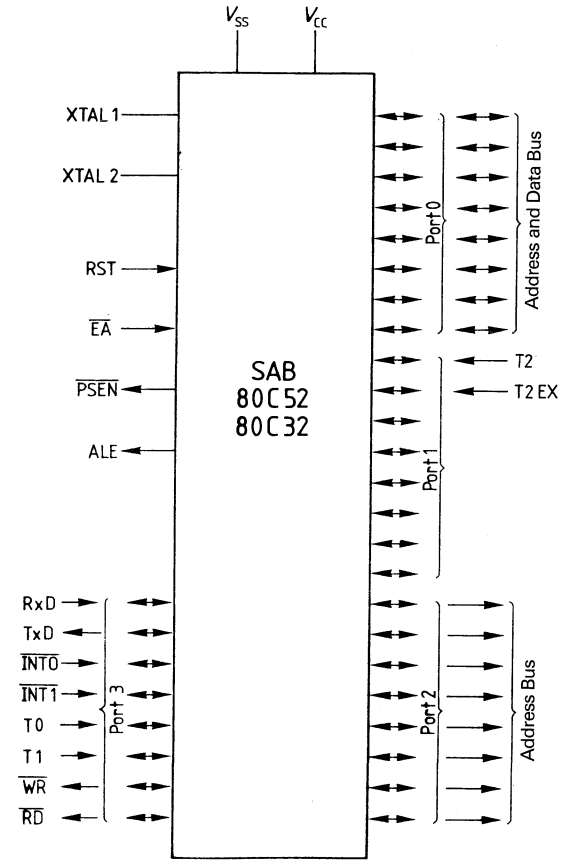
The SAB 80C52/80C32 is a standalone, high-performance CMOS single-chip microcontroller, designed in Siemens ACMOS technology. It is functionally compatible with the SAB 8052A/8032A devices in MYMOS technology.

Furthermore, it is backwardly compatible with the SAB 80C51/80C31. The low-power properties of ACMOS technology allow applications where power consumption and dissipation are critical. In addition, the SAB 80C52/80C32 has two software-selectable modes of reduced activity for further power reduction – idle and power-down.

The SAB 80C52 contains a non-volatile 8K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level interrupt structure, a serial I/O port, an on-chip oscillator, and clock circuits. The SAB 80C32 is identical, except that it lacks the program memory on the chip.

The SAB 80C52/80C32 is supplied in a 40-pin plastic dual-in-line (P-DIP-40) package, or a 44-pin plastic leaded chip carrier (PL-CC-44) package.

Logic Symbol



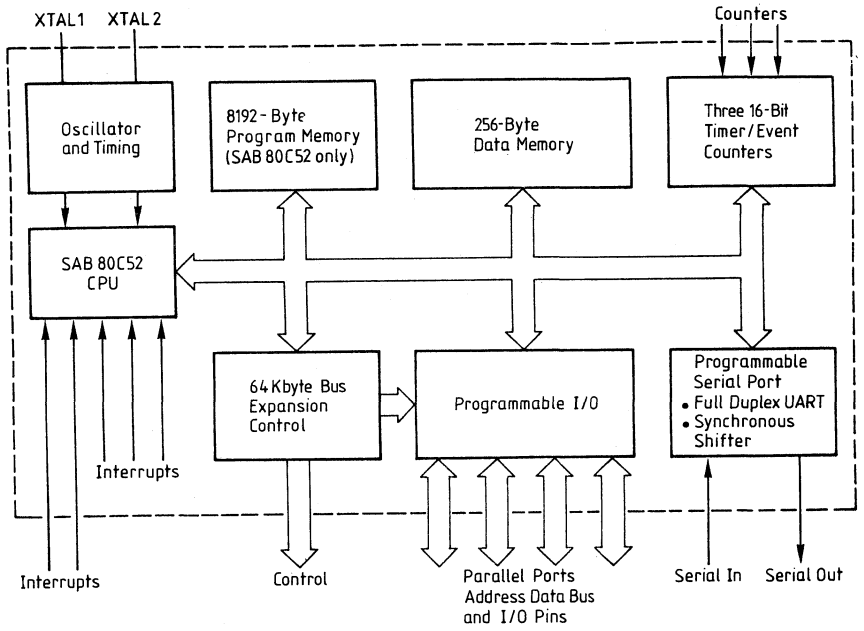
Pin Definitions and Functions

Symbol	Pin P-DIP40	Pin PLCC44	Input (I) Output (O)	Functions
P1.0–P1.7	1–8	2–9	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 1 also receives the low-order address bytes during program verification. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 EX (P1.1). Capture/Reload trigger of timer 2.
RST	9	10	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20		**XTAL 1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL2** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL 2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-DIP40	Pin PLCC44	Input (I) Output (O)	Functions
P2.0–P2.7	21–28	24–31	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resist. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	29	32	O	**$\overline{\text{PROGRAM STORE ENABLE}}$** This output issues a control signal that enables the external program memory to access the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	**ADDRESS LATCH ENABLE** Provides signal used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	31	35	I	**$\overline{\text{EXTERNAL ACCESS}}$** When held at a high level, the SAB 80C52 executes instructions from the internal ROM when the PC is less than 8192. When held at a low level, the SAB 80C52 fetches all instructions from the external program memory. For the SAB 80C32 this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C52. External pullup resistors are required during program verification.
V_{CC}	40	44		**Supply voltage** during normal, idle, and power-down operations.
V_{SS}	20	22		**Circuit ground potential**
NC	–	1, 12, 23, 34	–	**No connection**

Block Diagram



Functional Description

The SAB 80C52/80C32 is functionally compatible with the SAB 8052A/8032A products that are designed in Siemens MYMOS technology. Furthermore, the SAB 80C52/80C32 is backwardly compatible with the SAB 80C51/80C31 devices.

In addition, instead of the RAM backup power supply of the SAB 8052A/8032A, the SAB 80C52/80C32 offers two additional power control modes, the idle mode and the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

- Idle mode
  In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction that invokes the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The contents of the CPU, the on-chip RAM, and all the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor in the same way as a power-on reset.
- Power-down mode
  In the power-down mode the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. Only the contents of the on-chip RAM is preserved. A hardware reset is the only way to terminate power-down.

During power-down and idle mode the external pins will have the following status (see table 1):

Table 1
Status of the External Pins during Idle and Power-Down Modes

Mode	Program Memory	ALE	PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data/ Alternate Outputs	Data	Data/ Alternate Outputs
Idle	External	1	1	Float	Data/ Alternate Outputs	Address	Data/ Alternate Outputs
Power-Down	Internal	0	0	Data	Data/Last Output of Alternate Function	Data	Data/Last Output of Alternate Function
Power-Down	External	0	0	Float	Data/Last Output of Alternate Function	Data	Data/Last Output of Alternate Function

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A, ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 V to V_{CC} +0.5 V
Voltage on V_{CC} to V_{SS}	−0.5 to 6.5 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 20%; V_{SS} = 0 V; T_A = 0 to 70°C

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage (except EA)	V_{IL}	−0.5	$0.2V_{CC}-0.1$	V	–
Input low voltage (EA)	V_{IL1}	−0.5	$0.2V_{CC}-0.3$	V	–
Input high voltage (except XTAL1, RST)	V_{IH}	$0.2V_{CC}+0.9$	$V_{CC}+0.5$	V	–
Input high voltage (XTAL1, RST)	V_{IH1}	$0.7V_{CC}$	$V_{CC}+0.5$	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, PSEN)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4	–	V	I_{OH} = −60 µA V_{CC} = 5V ±10%
		$0.9V_{CC}$	–	V	I_{OH} = −10 µA
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4	–	V	I_{OH} = −400 µA V_{CC} = 5V ±10%
		$0.9V_{CC}$	–	V	I_{OH} = −40 µA [2]
Logical 0 input current (ports 1, 2, 3)	I_{IL}	–	−50	µA	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	–	−650	µA	V_{IN} = 2V
Input leakage current (port 0, EA)	I_{LI}	–	±10	µA	$0.45 < V_{IN} < V_{CC}$
Reset pulldown resistor	R_{RST}	50	150	kΩ	–
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25°C
Power down current	I_{PD}	–	50	µA	V_{CC} = 2 to 6V [3]

For notes refer to next page.

DC Characteristics (cont'd)

Maximum I_{CC} (mA)

	Active Mode [4]			Idle Mode [5]		
Freq. V_{CC}	4 V	5 V	6 V	4 V	5 V	6 V
0.5 MHz	TBD	TBD	TBD	TBD	TBD	TBD
3.5 MHz	TBD	TBD	TBD	TBD	TBD	TBD
8.0 MHz	TBD	TBD	TBD	TBD	TBD	TBD
12 MHz	TBD	24	TBD	TBD	10	TBD

Note [1]: Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading >100pF), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

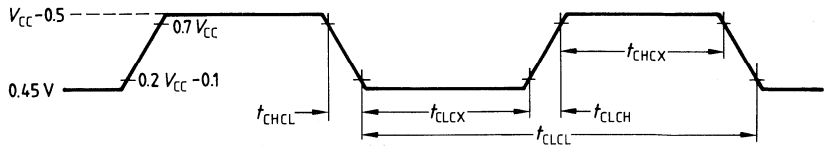
Note [2]: Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

Note [3]: Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = V_{CC}; XTAL1 = V_{SS}; XTAL2 = N.C.; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

Note [4]: I_{CC} (active mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = Port 0 = V_{CC}; $\overline{RESET}$ = V_{CC}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

Note [5]: I_{CC} (idle mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = V_{CC}; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode
$t_{CLCH} = t_{CHCL} = 5$ ns



AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±20%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}$-40	–	ns
Address setup to ALE	t_{AVLL}	28	–	t_{CLCL}-55	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL}-35	–	ns
ALE to valid instruction in	t_{LLIV}	–	234	–	$4t_{CLCL}$-100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	43	–	t_{CLCL}-40	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	205	–	$3t_{CLCL}$-45	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	145	–	$3t_{CLCL}$-105	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	59	–	t_{CLCL}-25	ns
Address to valid instruction in	t_{AVIV}	–	312	–	$5t_{CLCL}$-105	ns
$\overline{PSEN}$ to address float	t_{PLAZ}	–	10	–	10	ns

External Data Memory Characteristics

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL}$-100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL}$-100	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL}-35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL}$-165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL}$-70	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL}$-150	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL}$-165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	$4t_{CLCL}$-130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	23	–	t_{CLCL}-60	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL}-50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

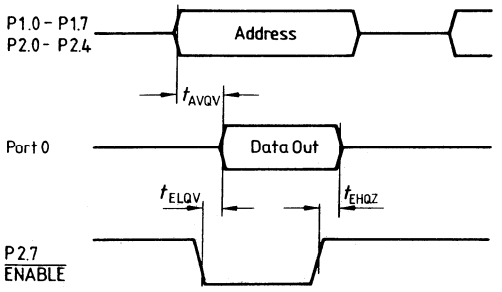
Parameter	Symbol	Limit values		Unit
		Variable clock Freq. = 0.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	2000	ns
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	12	MHz

ROM Verification Characteristics for SAB 80C52

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\,V \pm 20\%$; $V_{SS} = 0\,V$

Parameter	Symbol	Limit values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48\,t_{CLCL}$	ns
$\overline{\text{ENABLE}}$ to valid data	t_{ELQV}	–	$48\,t_{CLCL}$	ns
Data float after $\overline{\text{ENABLE}}$	t_{EHQZ}	0	$48\,t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification

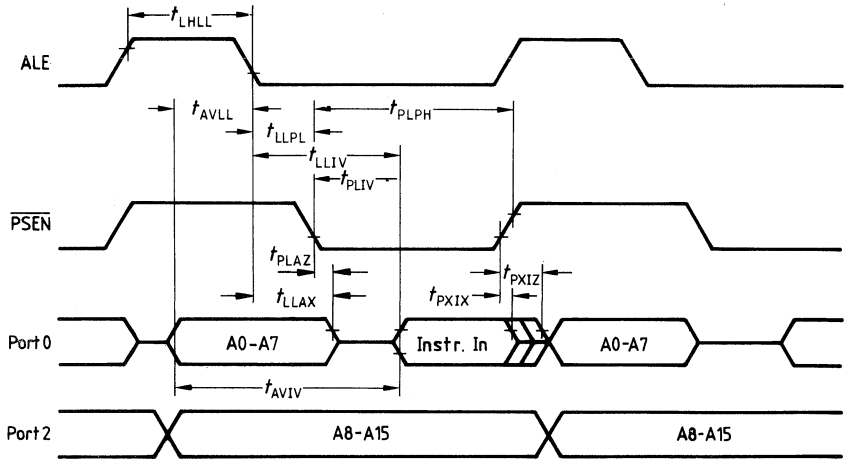


Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12
Data: Port 0 = D0–D7

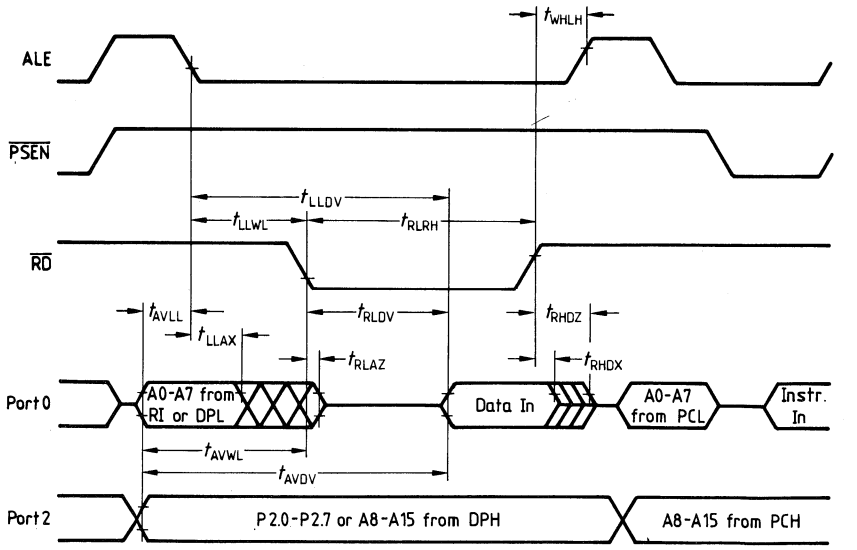
Inputs: P2.5–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
RST $= V_{IH1}$

Waveforms

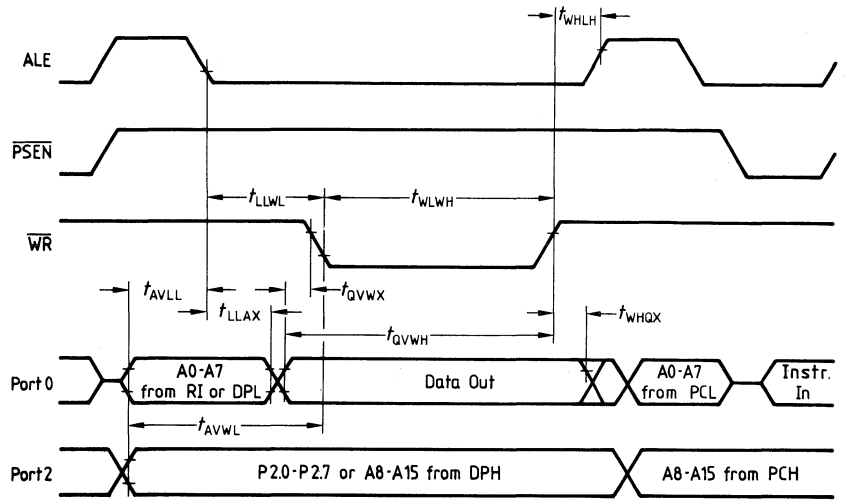
Program Memory Read Cycle



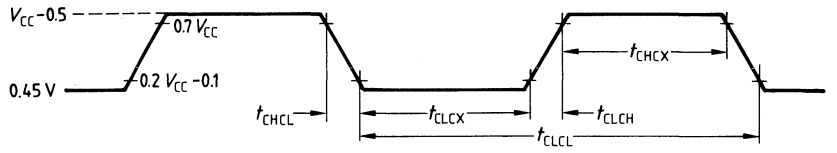
Data Memory Read Cycle



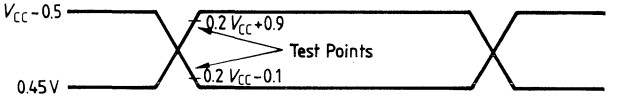
Data Memory Write Cycle



External Clock Cycle

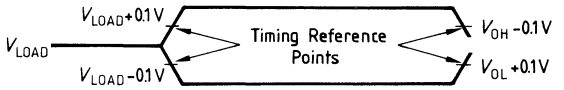


AC Testing: Input, Output Waveforms



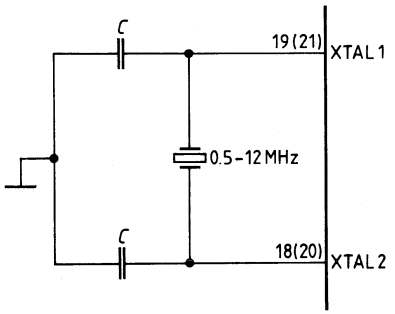
AC Inputs during testing are driven at V_{CC}-0.5V for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at $V_{IH\,min}$ for a logic '1' and $V_{IL\,max}$ for a logic '0'.

AC Testing: Float Waveforms



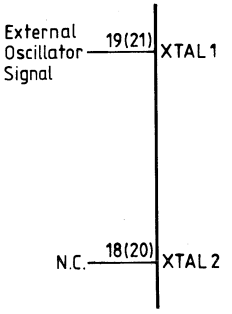
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

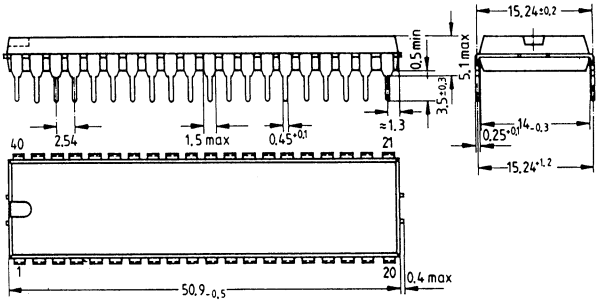
Crystal Oscillator Mode



Driving from External Source

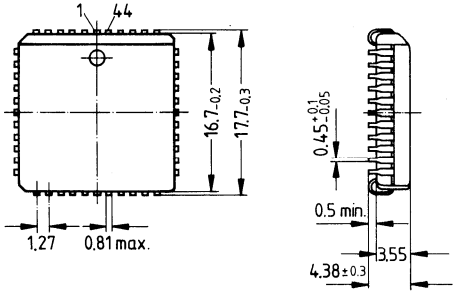
Pin numbers in (...) are for PLCC 44 package

40-Pin Plastic Package, P-DIP-40



Dimensions in mm

44-Pin Plastic Package, PL-CC-44



Dimensions in mm

Ordering Information

Type	Ordering code	Function
		8-bit CMOS microcontroller
SAB 80C52-P	Q 67120-C379	with mask-programmable ROM (P-DIP-40)
SAB 80C32-P	Q 67120-C378	for external memory (P-DIP-40)
SAB 80C52-N	Q67120-C396	with mask-programmable ROM (PL-CC-44)
SAB 80C32-N	Q67120-C395	for external memory (PL-CC-44)

Telephone Controller (Single-Chip 8-Bit CMOS Microcontroller)

SAB 80C482
SAB 80C382

Preliminary Data **CMOS IC**

The SAB 80C482 is a low-power, advanced CMOS member of the popular SAB 8048 family. The SAB 80C482 contains double-sized program memory and 4 additional I/O lines. For systems that require extra capability, the SAB 80C482 can easily be expanded using CMOS external memories. The on-chip mask-programmable keyboard wake-up offers a convenient solution for a power-saving keyboard scanner. The SAB 80C482 has the same cycle time at about half the SAB 8048 clock frequency. The 100% static operation provides the possibility to optimize between power consumption and program speed.

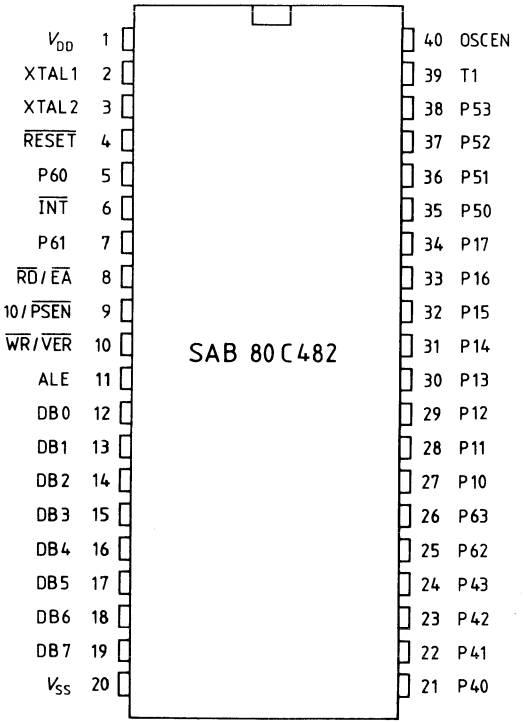
The CMOS design of the SAB 80C482 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions. These applications include telecommunications, automotive, consumer, portable, and hand-held instruments.

The SAB 80C382 is the ROM-less version of the SAB 80C482

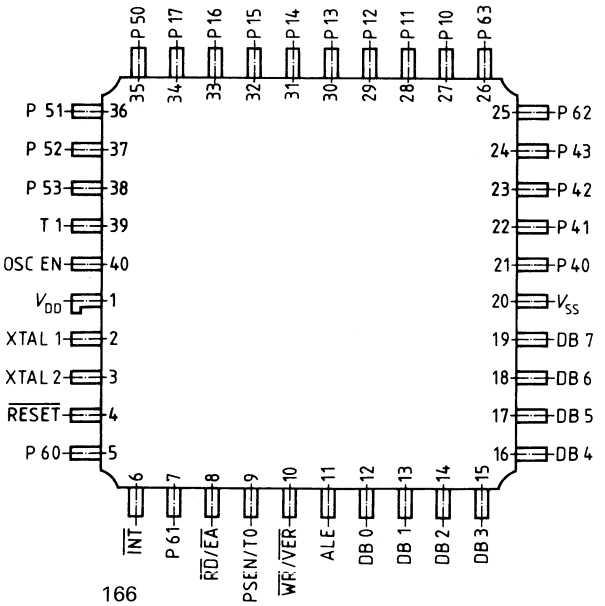
- 2K × 8 ROM
- 64 × 8 RAM
- 31 I/O lines
- 2.66 µs cycle time (with 3 MHz crystal)
- Automatic power-on reset
- Keyboard wake-up
- Very low power consumption
- Normal: 1.0 mA@5 V@8 µs cycle
- Halt: 0.4 mA@5 V@8 µs cycle
- Standby: 1 µA@5 V
- 100% static operation
- Supply voltage: 2.5 to 6 V

5.87

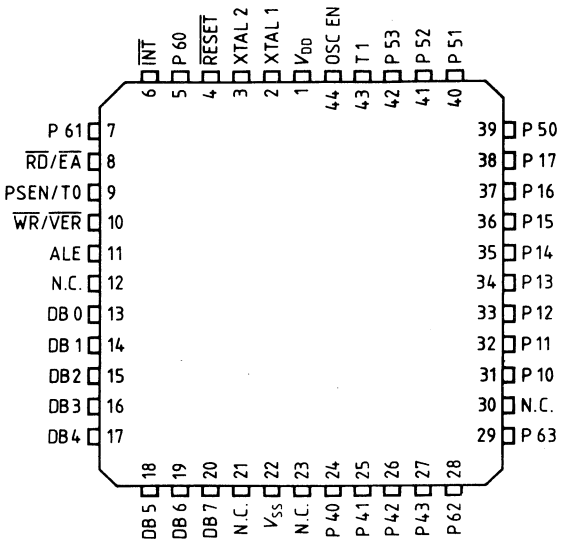
Pin Configurations
(top view)
P-DIP 40



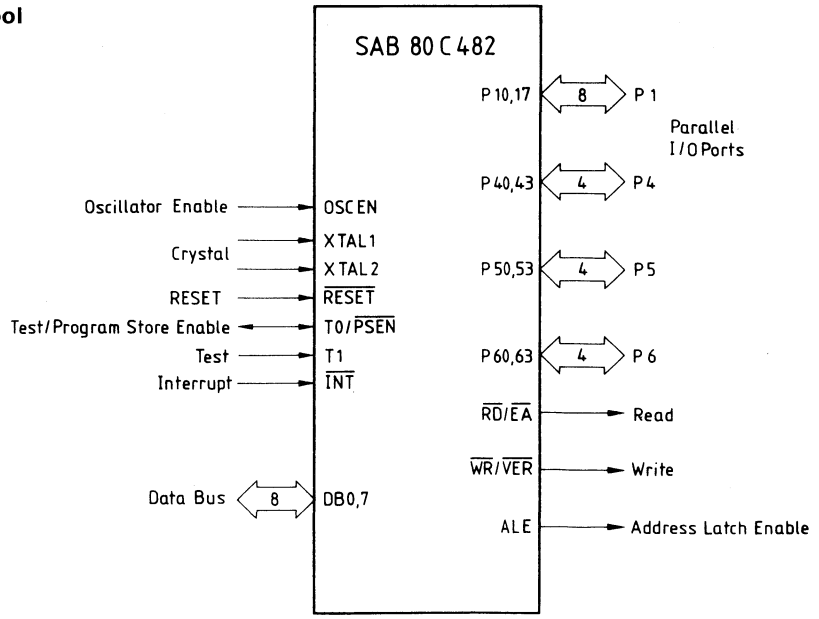
MIKROPACK



Pin Configuration
(top view)
PLCC 44



Logic Symbol



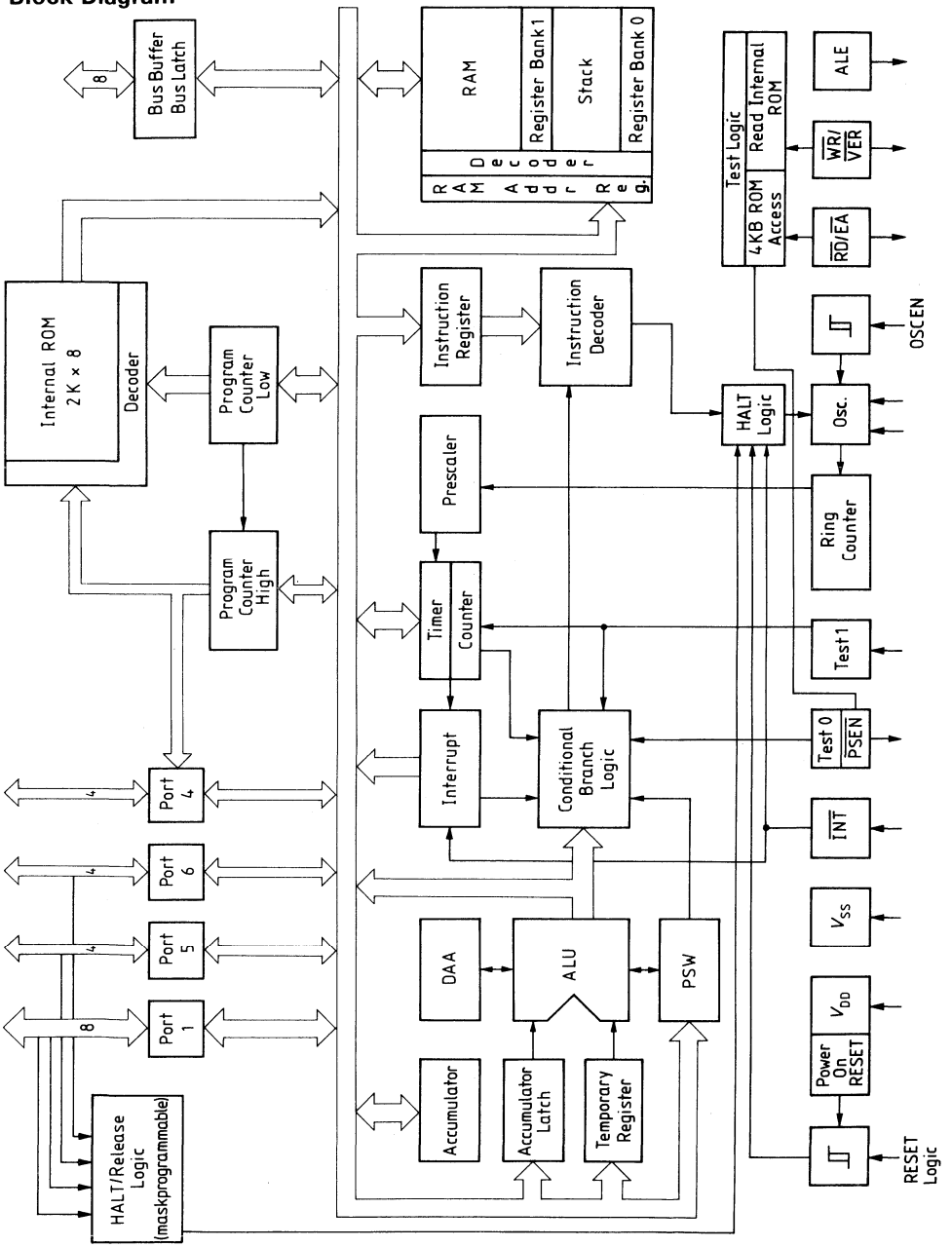
Pin Description

PLCC	P-DIP 40 MIKROPACK	Symbol	Description
2	2	XTAL1	Oscillator input; one side of crystal input also input for external frequency source
3	3	XTAL2	Oscillator output; other side of crystal input. This pin is not connected when an external frequency source is used.
44	40	OSCEN	Oscillator enable input (Schmitt-Trigger input) A high signal enables oscillator to run. A low signal stops oscillator and initializes standby mode.
4	4	$\overline{\text{RESET}}$	Input used to initialize processor (active low). (Schmitt-Trigger input)
6	6	$\overline{\text{INT}}$	Interrupt input with internal pull-up resistor. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after reset. HALT mode is terminated by interrupt (active low).
8	8	$\overline{\text{RD}}/\overline{\text{EA}}$	Output strobe activated during a bus read. Can be used to enable transfer of data on the bus from an external device. Used a read strobe to external data memory (active low). External access input which forces all program memory fetches to reference external memory. Active only during the initialization time (RESET at low)! (active low).
9	9	T0/$\overline{\text{PSEN}}$	Input pin testable using the instructions JT0 and JNT0 until disabled through an execution of instructions SEL MB0 or SEL MB1. Program store enable. This output is enabled through the first execution of instructions SEL MB0 or SEL MB1. It can be disabled only through a new RESET initialization. It occurs only during a fetch to external program memory (active low).
10	10	$\overline{\text{WR}}/\overline{\text{VER}}$	Output strobe during a bus write. Used as write strobe to external data memory (active low). ROM verification input is low during the whole time. The contents of the internal ROM can be read without program execution.

Pin Description (cont'd)

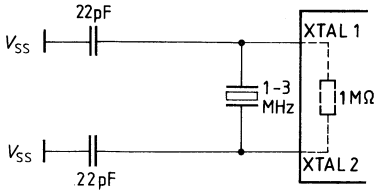
PLCC	P-DIP 40 MIKROPACK	Symbol	Description
11	11	ALE	Address latch enable. This signal occurs once during each cycle and is useful as clock output. Negative edge of ALE strobes address into external data and program memory.
13...20	12...19	DB0...DB7	True bidirectional port which can be written or read synchronously using WR, RD strobes. Contains the 8 low-order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.
24...27	21...24	P40...P43	4-bit quasi-bidirectional port. Internal pull-up resistors. This port contains the four high order program-counter bits during an external program memory fetch.
5, 7	5, 7	P60...P63	4-bit quasi-bidirectional port. Internal pull-up resistors.
28, 29	25, 26		Keyboard wake-up capability mask-programmable.
31...38	27...34	P10...P17	8-bit quasi bidirectional port. Internal pull-up resistors. Keyboard wake-up capability mask-programmable.
39...42	35...38	P50...P53	4-bit quasi-bidirectional port. Internal pull-up resistors. Keyboard wake-up capability mask-programmable.
43	39	T1	Input pin testable using JT1, and JNT1 instructions. Can be designated as timer/counter input using the STRT CNT instuction.
1	1	V_{DD}	Power supply
22	20	V_{SS}	Circuit GND potential (0 V)
12, 21	–	N.C.	Not connected
23, 30	–	N.C.	Not connected

Block Diagram

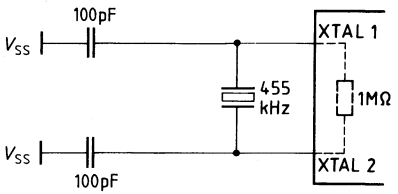


Oscillator

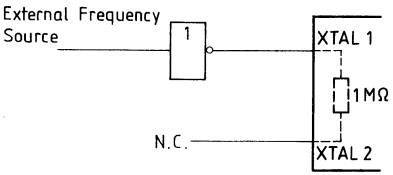
The on-board oscillator is a high-gain resonant circuit with a frequency range between 0 and 3 MHz. The clock frequency is determined by the resonator (e.g. crystal) connected between the pins XTAL1 and XTAL2.



a) Crystal Wiring



b) Ceramic Oscillator



c) External Clock Generator

8-Bit Timer/Counter

The SAB 80C842 contains a timer/counter to aid the user in counting and generating accurate time delays without placing a burden on the processor for these functions.

Timer

Execution of a START T instruction connects an internal clock to the counter input. The XTAL frequency divided by 256 is the timer input frequency.

Counter

Execution of a START CNT instruction connects the T1 pin to the counter input and enables the counter. Subsequent high-to-low transition on T1 pin must be held low for at least one machine cycle to ensure it is not missed. The counter may be incremented only once throughout three instruction cycles. There is no minimum frequency limit.

Program Memory

The resident program memory consists of 2048 bytes. There are three particulary important locations in program memory:

1. **Location 0:**
   Executing the initialization reset causes the first instruction to be fetched from location 0.
2. **Location 3:**
   Execution starts at location 3 after the interrupt input (pin 6) of the processor has gone low (if interrupt is enabled).
3. **Location 7:**
   A timer/counter interrupt resulting from timer/counter overflow (if enabled).

Program Memory Configurations

1. **Internal 2 Kbyte ROM**
   - pin 9 is available as T0 input
   - port 4 serves only as I/O port
2. **Internal 2 Kbyte ROM and additional, external 2 Kbyte ROM**
   - with external access, instruction words are read in via bus (data bus, DB).
   - an SEL MB0 or an SEL MB1 instruction must be executed before using the data bus for external program store access.
   - execution of SEL MB1 instruction followed by CALL or JMP enables exceeding internal 2 Kbyte limits and accessing of external ROM.
   - external program memory access causes loading of program counter bits PC8 through PC11 at port lines 40 to 43. PC0 through PC7 appear on bus during the falling edge of ALE.
   - execution of MOVP3 A,@A instruction causes internal ROM (bank 0) to be selected.
   - internal ROM is automatically selected during every execution of an interrupt service routine.
   - in second cycle of MOVX instruction no $\overline{\text{PSEN}}$ signal appears and $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal is active. Port 4 is not affected.
3. **External 4 Kbyte ROM, internal ROM disabled**
   - sole access to external 4 Kbyte ROM is initiated by logic 0 at pin 8 ($\overline{\text{RD}}/\overline{\text{EA}}$) during initialization time (RESET at low). At the machine cycle T8 test logic calls up status from pin 8.
   - pin 9 serves as $\overline{\text{PSEN}}$ output.
   - program counter bits PC0 through PC7 appear at DB0 through DB7 and PC8 through PC11 appear at port lines P40 through P43.
   - execution of MOVP3 A,@A instruction or interrupt routine selects automatically lower 2 Kbytes of external ROM.

4. Internal ROM verification without program execution

- pin 10 ($\overline{WR}/\overline{VER}$) must be low during the whole verification time. The low level at this pin forces the SAB 80C482 to the verification mode.
- contents of internal ROM appear on lines DB0 through DB7
- program-counter bits PC0 through PC7 appear at DB0 through DB7 and PC8 through PC11 at port lines P40 through P43.
- ALE and $\overline{PSEN}$ are enabled.

Reset

The reset signal sets the microcomputer to a defined initial state. There are two possibilities to reach this state.

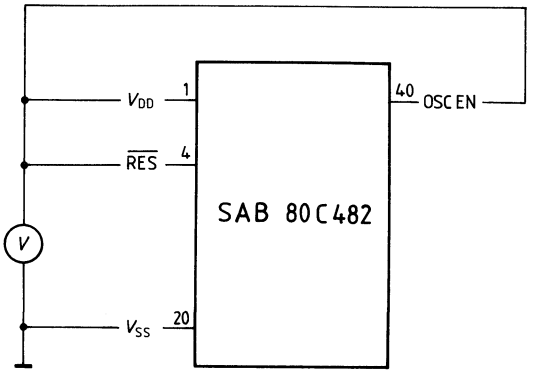
1. by an external signal at pin 4 (RESET)
2. by an internal signal generated through the built-in power-on-reset circuit.

If the oscillator is enabled (OSCEN at high), reset performs the following functions:

1. sets program counter to zero (PC = 000H)
2. sets stack pointer to zero (SP = 00H)
3. selects register bank 0
4. selects memory bank 0 (internal ROM)
5. sets bus to high impedance state
   (except when $\overline{RD}/\overline{EA}$ or $\overline{WR}/\overline{VER}$ is at low)
6. sets ports 1, 4, 5, 6 to input mode
7. stops counter/timer
8. enables pin 9 as test input T0
9. disables interrupts
10. clears timer flag
11. releases HALT mode
12. does not affect internal RAM contents

Timing diagrams for power-on and external reset are shown in fig. a) and b).

Figure a) Internal Power-On Reset



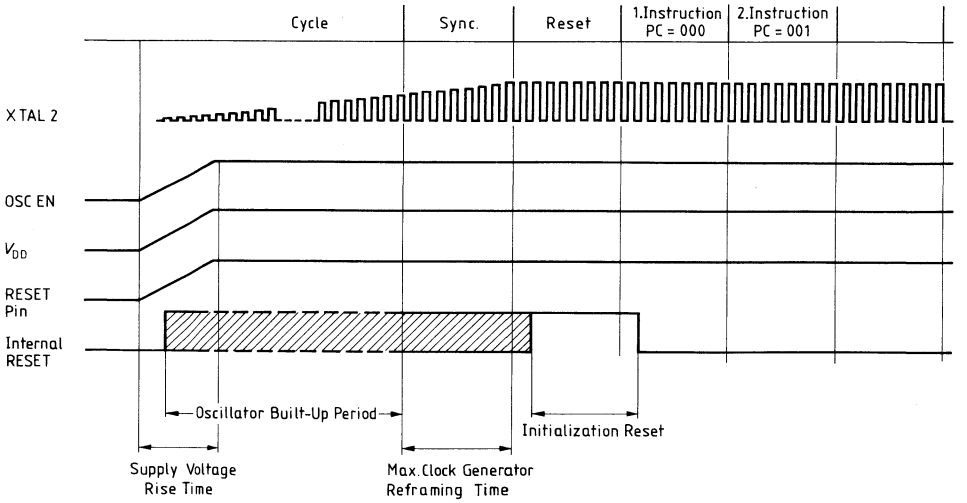
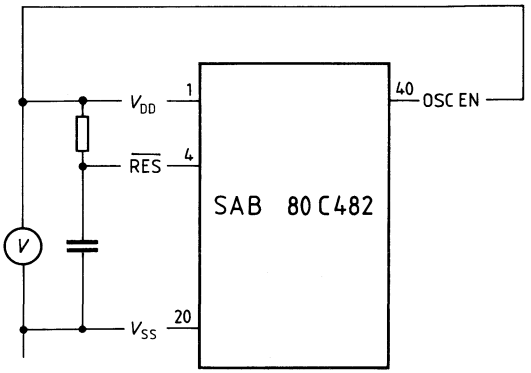
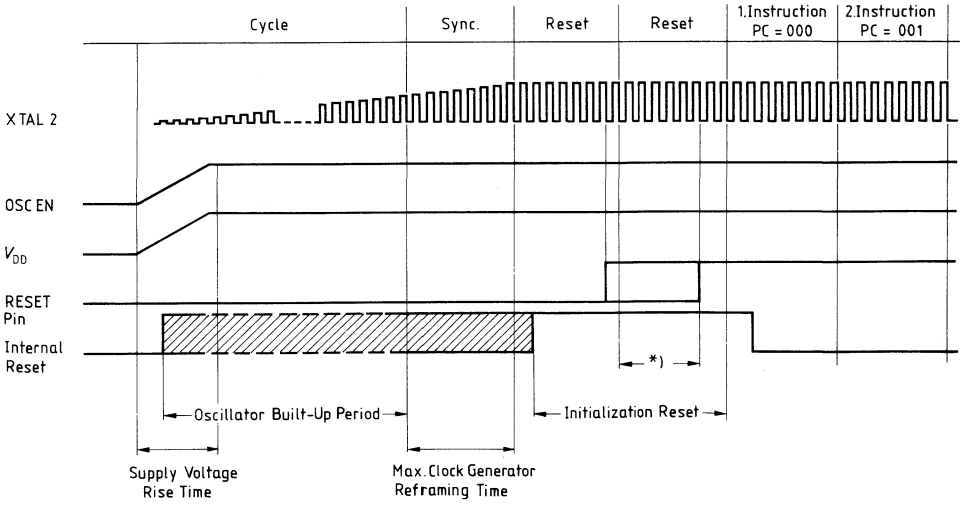


Figure b) External Reset





*) During this Time-Slot the Signal at Reset-Pin Can Change to V_{DD} without Lengthening the Reset Execution

Interrupt

The SAB 80C482 has the same interrupt logic as the SAB 8048. The interrupt can be initialized through two possible sources:

1. external low active signal at pin $\overline{\text{INT}}$
2. overflow of the internal counter/timer.

Keyboard Wake-Up

The SAB 80C482 has a special on-chip circuitry for a convenient keyboard-scanning named "Keyboard Wake-Up". Four NAND gates can be connected the ports P10–13, P14–17, P50–53 and P60–63 by mask programming. Ports 5 and 6 are already connected in standard version. The outputs of these gates are interconnected in the NOR manner. The resulting output controls the release from the HALT mode.

This means, the SAB 80C482 can be "waked up" on any keystroke without the necessity of using a double contact keyboard.

HALT Mode

After execution of the HALT instruction the processor enters the HALT mode where the internal clocks and internal logic are disabled. The oscillator is running. In the HALT mode, power consumption is about 1/3 of normal SAB 80C482 operation.

HALT mode can be released in three different ways:

1. by low pulse on the $\overline{\text{RESET}}$ pin
   (program starts at address location 0)
2. via keyboard wake-up
   (program continues at address location PC+1)
3. by low pulse on the $\overline{\text{INT}}$ pin
   (if interrupt is enabled the interrupt subroutine starting at the address location 3 is executed. After its execution, or if interrupt is disabled, program continues at address location PC+1.)

Standby

Standby provides additional, drastic power consumption savings over the HALT mode.

Standby is initiated by forcing the OSCEN pin to low state. Oscillator operation is discontinued. While in standby, the following data is maintained:

1. internal RAM
2. stack pointer
3. program counter
4. memory bank status
5. T0/$\overline{\text{PSEN}}$ status
6. I/O status on all ports
7. all internal logic states

It is possible, but not recommended, to put the SAB 80C482 on standby without regard to the running program. Stopping at any time in the instruction cycle can result in an undefined status. Consequently, it is advisable to enter standby only from the HALT state or if an external reset signal is applied. The $\overline{\text{RES}}$ pin must be forced at least 2.5 cycles earlier to the low level than the OSCEN pin.

If the SAB 80C482 has entered the standby from the HALT mode, it is still in the HALT mode after the OSCEN pin has been forced high. In the second case, the $\overline{\text{RES}}$ pin has to be held at least for the oscillator built-up period plus one cycle at low level after the OSCEN pin has been forced high.

Instruction Set

There are five new instructions in addition to the SAB 8048 instruction set:

DEC	@ R0	instruction code	C0
DEC	@ R1	instruction code	C1
DJNZ	@ R0, addr	instruction code	E0
DJNZ	@ R1, addr	instruction code	E1
HALT		instruction code	F3

The following SAB 8048 instructions are not available:

IN	A, P2	instruction code	0A
MOVD	A, P7	instruction code	0F
OUTL	P2, A	instruction code	3A
MOVD	P7, A	instruction code	3F
ENTO	CLK	instruction code	75
JF1	addr	instruction code	76
CLR	F0	instruction code	85
ORL	P2, # data	instruction code	8A
ORLD	P7, A	instruction code	8F
CPL	F0	instruction code	95
ANL	P2, # data	instruction code	9A
ANLD	P7, A	instruction code	9F
CLR	F1	instruction code	A5
CPL	F1	instruction code	B5
JF0	addr	instruction code	B6
MOV	A, PSW	instruction code	C7
MOV	PSW, A	instruction code	D7

The opcode of the following instruction has been changed:

JNI	addr	instruction code	66 (8048 = 86)

Symbols and Abbreviations

A	Accumulator
AC	Auxiliary carry
addr	Program memory address
An	Accumulator bit n
Bb	Bit designator b = 0 to 7
BS	Bank switch
BUS	Bus port
CY	Carry
CLK	Clock
CNT	Event counter
data	8-Bit number or expression
MBF	Memory bank flipflop
I	Interrupt
PC	Program counter
Pp	Port designator p = 4 to 6
P1	Port 1
PSW	Program status word
Ri	Register designator i = 0, 1
Rr	Register designator r = 0 to 7
SP	Stack pointer
T	Timer
TF	Timer/counter flag
T0/T1	Test 0, test 1
X	Mnemonic for external RAM
#	Immediate data prefix
@	Indirect address prefix
(X)	Contents of X
((X))	Contents of location addressed by (X)
←	Is replaced by
↔	Is exchanged with
AND	Logical AND operation
OR	Logical OR operation
XOR	Logical EXOR operation

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Accumulator and Register Move Instructions						
MOV A, Rr	(A) ← (Rr)	Move register to accumulator	F8–FF		1	1
MOV A, @ Ri	(A) ← ((Ri))	Move data memory to accumulator	F0–F1		1	1
MOV A, # data	(A) ← data	Move data to accumulator	23		2	2
MOV Rr, A	(Rr) ← (A)	Move accumulator to register	A8–AF		1	1
MOV @ Ri, A	((Ri)) ← (A)	Move accumulator to data memory	A0–A1		1	1
MOV Rr, # data	(Rr) ← data	Move data to register	B8–BF		2	2
MOV @ Ri, # data	((Ri)) ← data	Move data to data memory	B0–B1		2	2
MOVX A, @ Ri	(A) ← ((Ri))	Move external data to accumulator	80–81		1	2
MOVX @ Ri, A	((Ri)) ← (A)	Move accumulator to external data memory	90–91		1	2
XCH A, Rr	(A) ↔ (R)	Exchange register and accumulator	28–2F		1	1
XCH A, @ Ri	(A) ↔ ((Ri))	Exchange data memory and accumulator	20–21		1	1
XCHD A, @ Ri	(A0–3) ↔ ((Ri0–3))	Exchange nibble of data memory and accumulator	30–31		1	1
MOVP3 A, @ A	save (PC) (PC0–7) ← (A) (PC8–11) ← 011 B (A) ←((PC)) restore PC	Move data from page 3 of program memory to accumulator	E3		1	2
MOVP A, @ A	save (PC) (PC0–7) ← (A) (A) ← ((PC)) restore PC	Move data from current page of program to accumulator	A3		1	2
SWAP A	(A4–7) ↔ (A0–3)	Exchange accumulator nibbles	47		1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Timer/Counter Move Instructions						
MOV A, T	(A) ← (T)	Read counter/timer into accumulator	42		1	1
MOV T, A	(T) ← (A)	Load counter/timer from accumulator	62		1	1
Port Move Instructions						
IN A, P1	(A) ← (P1)	Move data at port 1 to accumulator	09		1	2
OUTL P1, A	(P1) ← (A)	Output accumulator on port 1	39		1	2
ANL P1, # data	(P1) ← (P1) AND data	Logical AND port 1 with data	99		2	2
ORL P1, # data	(P1) ← (P1) OR data	Logical OR port 1 with data	89		2	2
IN A, BUS	(A) ← (BUS)	Move data on bus to accumulator	08		1	2
OUTL BUS, A	(BUS) ← A	Output accumulator on bus	02		1	2
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical AND bus with data	98		2	2
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical OR bus with data	88		2	2
MOVD A, Pp	(A0–3) ← (Pp) (A4–7) ← 0	Move data at port 4 – 6 to accumulator	OC–OE		1	2
MOVD Pp, A	(Pp) ← (A0–3)	Output accumulator on port 4 – 6	3C–3E		1	2
ANLD Pp, A	(Pp) ← (A0–3) AND (Pp)	Logical AND accumulator with port 4 – 6	9C–9E		1	2
ORLD Pp, A	(Pp) ← (A0–3) OR (Pp)	Logical OR accumulator with port 4 – 6	8C–8E		1	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Arithmetic Accumulator Instructions						
ADD A, Rr	(A) ← (A) + (Rr)	Add register to accumulator	68–6F	AC CY	1	1
ADD A, @ Ri	(A) ← (A) + ((Ri)	Add data memory to accumulator	60–61	AC CY	1	1
ADD A, # data	(A) ← (A) + data	Add data to accumulator	03	AC CY	2	2
ADDC A, Rr	(A) ← (A) + (Rr) + (CY)	Add register and carry to accumulator	78–7F	AC CY	1	1
ADDC A, @ Ri	(A) ← (A) + ((Ri)) + (CY)	Add data memory and carry to accumulator	70–71	AD CY	1	1
ADDC A, # data	(A) ← (A) + data + (CY)	Add data and carry to accumulator	13	AC CY	2	2
INC A	(A) ← (A) + 1	Increment accumulator by 1	17		1	1
DEC A	(A) ← (A) – 1	Decrement accumulator by 1	07		1	1
DA A		Decimal adjust accumulator	57	CY	1	1
Arithmetic Register Instructions						
INC Rr	(Rr) ← (Rr) + 1	Increment register by 1	18–1F		1	1
DEC Rr	(Rr) ← (Rr) – 1	Decrement register by 1	C8–CF		1	1
DEC @ Ri	((Ri)) ← ((Ri)) ← ((Ri)) – 1	Decrement data memory by 1	C0–C1		1	1
INC @ Ri	((Ri)) ← ((Ri)) + 1	Increment data memory by 1	10–11		1	1
DJNZ Rr, addr	(Rr) ← (Rr) – 1 if (Rr) ≠ 0 (PC0–7)←addr	Decrement register by 1 and jump if register not zero	E8–EF		2	2
DJNZ @ Ri, addr	((Ri)) ← ((Ri)) – 1 if ((Ri)) ≠ 0 (PC0–7)←addr	Decrement data memory by 1 and jump if data memory is not zero	E0–E1		2	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Logical Accumulator and Register Instructions						
ANL A, Rr	(A) ← (A) AND (Rr)	Logical AND accumulator with register	58–5F		1	1
ANL A, @ Ri	(A) ← (A) AND ((Ri))	Logical AND accumulator with data memory	50–51		1	1
ANL A, # data	(A) ← (A) AND data	Logical AND accumulator with data	53		2	2
ORL A, Rr	(A) ← (A) OR (Rr)	Logical OR accumulator with register	48–4F		1	1
ORL A, @ Ri	(A) ← (A) OR ((Ri))	Logical OR accumulator with data memory	40–41		1	1
ORL A, # data	(A) ← (A) OR data	Logical OR accumulator with data	43		2	2
XRL A, Rr	(A) ← (A) XOR (Rr)	Logical XOR accumulator with register	D8–DF		1	1
XRL A, @ Ri	(A) ← (A) XOR ((Ri))	Logical XOR accumulator with data memory	D0–D1		1	1
XRL A, # data	(A) ← (A) XOR data	Logical XOR accumulator with data	D3		2	2
CLR A	(A) ← 0	Clear accumulator	27		1	1
CPL A	(A) ← $(\overline{A})$	Complement accumulator	37		1	1
Rotate Instructions						
RL A	(An+1) ← (An)	Shift accumulator 1 bit to left	E7		1	1
RLC A	(An+1) ← (An) (CY) ← (A7) (A0) ← (CY)	Shift accumulator 1 bit to left through carry	F7	CY	1	1
RR A	(An) ← (An+1)	Shift accumulator 1 bit to right	77		1	1
RRC A	(An) ← (An+1) (CY) ← (A0) (A7) ← (CY)	Shift accumulator 1 bit to right through carry	67	CY	1	1
Flag Instructions						
CLR C	(CY) ← 0	Clear carry bit	97	CY	1	1
CPL C	(CY) ← $(\overline{CY})$	Complement carry bit	A7	CY	1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Branch Instructions						
JMP addr	(PC0–7) ← addr 0–7 (PC8–10) ← addr 8–10 (PC11) ← DBF	Jump to address, page 0 1 2 3 4 5 6 7	 04 24 44 64 84 A4 C4 E4		 2 2 2 2 2 2 2 2	 2 2 2 2 2 2 2 2
JMPP @ A	(PC0–7) ← ((A))	Jump to address defined in program memory	B3		1	2
JC addr	if (CY) = 1 (PC0–7) ← addr	Jump to address if carry = 1	F6		2	2
JNC addr	if (CY) = 0 (PC0–7) ← addr	Jump to address if carry = 0	E6		2	2
JZ addr	if (A) = 0 (PC0–7) ← addr	Jump to address if accumulator = 0	C6		2	2
JNZ addr	if (A) > 0 (PC0–7) ← addr	Jump to address if accumulator > 0	96		2	2
JT0 addr	if T0 = 1 (PC0–7) ← addr	Jump to address if T0 is High	36		2	2
JNT0 addr	if T0 = 0 (PC0–7) ← addr	Jump to address if T0 is Low	26		2	2
JT1 addr	if T1 = 1 (PC0–7) ← addr	Jump to address if T1 is High	56		2	2
JNT1 addr	if T1 = 0 (PC0–7) ← addr	Jump to address if T1 is Low	46		2	2
JTF addr	if TF = 1 (PC0–7) ← addr (TF) ← 0	Jump to address if counter/timer flag = 1	16	TF	2	2
JNI addr	if $\overline{INT}$ = 0 (PC0–7) ← addr	Jump to address if interrupt input Low	66		2	2
JBb addr	if (An) = 1 (PC0–7) ← addr	Jump to address, n=0 if bit n of 1 accumulator = 1 2 3 4 5 6 7	12 32 52 72 92 B2 D2 F2		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Subroutine Instructions						
CALL addr	((SP)) ← (PC0–11, PSW4–7) (SP) ← (SP)+1 (PC0–10) ← addr 0–10 (PC11) ← DBF	Jump to page 0 subroutine 1 2 3 4 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
RET	(SP) ← (SP)–1 (PC) ← ((SP))	Return without PSW Restore	83		1	2
RETR	(SP) ← (SP)–1 (PC) ← ((SP)) (PSW4–7) ← ((SP))	Return with PSW Restore	93	CY AC DBF	1	2
Control Instructions						
STRT T		Start timer	55		1	1
STRT CNT		Start counter	45		1	1
STOP TCNT		Stop timer/counter	65		1	1
EN TCNTI		Enable timer/ counter interrupt	25		1	1
DIS TCNTI		Disable timer/ counter interrupt	35		1	1
EN I		Enable external interrupt	05		1	1
DIS I		Disable external interrupt	15		1	1
SEL RB0		Select register bank 0	C5	BS	1	1
SEL RB1		Select register bank 1	D5	BS	1	1
SEL MB0		Select program-memory bank 0	E5	DBF	1	1
SEL MB1		Select program-memory bank 1	F5	DBF	1	1
NOP		No operation	00		1	1
HALT		HALT instruction	F3		1	1

Maximum ratings

Ambient temperature under bias	T_A	−10 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Supply voltage ref. to GND (V_{ss})	V_{DD}	0.3 to 7	V
Total power dissipation	P_{tot}	1	W
All input and output voltages		−0.8 to V_{DD} +0.8	V

DC characteristics

T_A = −10 to 70°C; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V

		Test conditions	min.	typ.	max.	Unit
L input voltage	V_{IL}		−0.5		0.75	V
H input voltage	V_{IH}		0.7 x V_{DD}		V_{DD}+0.5	V
L output voltage	V_{OL}	I_{OL} = 1.0 mA			0.45	V
H output voltage	V_{OH}	I_{OH} = −1.0 mA	0.75 x V_{DD}			V
Input leakage current	I_{IL}	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
Input current XTAL	I_{XT}	$V_{SS} \le V_{IN} \le V_{DD}$	±9		±12	µA
Input current Ports, $\overline{INT}$ (Pull-up)	I_{ILP}	$V_{SS} \le V_{IN} \le V_{IL}$	−4		−7	µA
Input current $\overline{RD}$, $\overline{WR}$ (Normaly output)	I_{RW}	$V_{SS} \le V_{IN} \le V_{IL}$			−11	mA
Output leakage current (Bus and $\overline{PSEN}$ TO in high impedance states)	I_{OL}	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
Total supply current	I_{DD}	3 MHz; 5 V	3.1	550	3.75	mA
		1 MHz; 5 V	1.0		1.4	mA
		500 kHz; 5 V	0.7	250	0.9	mA
		$V_{SS} \le V_{IL} \le 0.4$ V				
		4.8 V $\le V_{IH} \le V_{DD}$				
HALT supply current	I_{DDH}	3 MHz; 5 V		1		µA
		1 MHz; 5 V			400	µA
		500 kHz; 5 V				µA
		$V_{SS} \le V_{IL} \le 0.4$ V				
		$4.8 \le V_{IH} \le V_{DD}$				
Standby current	I_{DDS}	V_{DD} = 5 V			2	µA
		$V_{SS} \le V_{IL} \le 0.4$ V				
		$4.8 \le V_{IH} \le V_{DD}$				
Operation supply voltage	V_{DD}		2.5		6	V
Data retention voltage	V_{DDR}		1.2			V

AC characteristics

T_A = –10 to 70°C; V_{DD} = 5 V; V_{SS} = 0 V; f_{OSC} = 3 MHz
C_L = 40 pF

		Test conditions	min.	typ.	max.	Unit
ALE pulse width	t_{LL}		400			ns
Address set-up before ALE	t_{AL}		20	45		ns
Address hold from ALE	t_{LA}		50		160	ns
Control pulse width						
$\overline{PSEN}$	t_{CC}		300	333		ns
$\overline{RD}$, $\overline{WR}$	t_{CC}		1300	1333		ns
Data set-up before $\overline{WR}$	t_{DW}		1300	1333		ns
Data hold after $\overline{WR}$	t_{WD}	t_{CY} = 2.66 µs C_L = 40 pF	300	333		ns
Cycle time	t_{CY}		2.66			µs
Data hold after $\overline{RD}$	t_{DR}		0		300	ns
Instr. hold after $\overline{PSEN}$	t_{DR}		0		300	ns
$\overline{RD}$ to data in	t_{RD}				1000	ns
$\overline{PSEN}$ to data in	t_{RD}				100	ns
Address set-up before $\overline{WR}$	t_{AW}		1900			ns
Address set-up to data						
at $\overline{RD}$	t_{AD}				3300	ns
at $\overline{PSEN}$	t_{AD}				400	ns
Address float to						
$\overline{RD}$	t_{AFC}		166	333		ns
$\overline{PSEN}$	t_{AFC}		50	100		ns
$\overline{WR}$ to ALE	t_{CA}		600			ns
$\overline{PSEN}$ to ALE	t_{CA}		1600			ns
ALE to $\overline{RD}$	t_{CA}		250			ns
ADDRESS Time Port 4	t_{ADD}		600			ns

Time Parameters versus f_{OSC}

Symbol	Parameter	
t	$1/f_{OSC}$	µs
t_{CY}	8 t	µs

Read from external data memory

t_{LL}	1.5 t	µs
t_{CA}	1.0 t	µs
t_{AFC}	1.0 t	µs
t_{CC}	4.0 t	µs
t_{DR}	–	µs
t_{RD}	3.5 t	µs
t_{AD}	10.5 t	µs

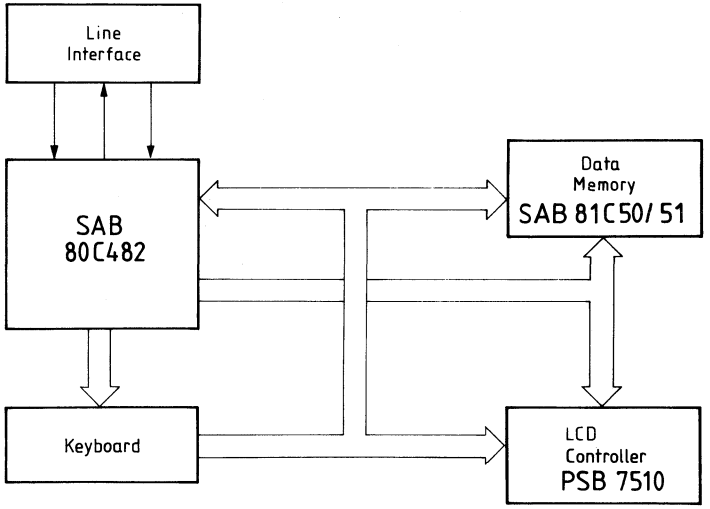
Write into external data memory

t_{CA}	2.0 t	µs
t_{CC}	4.0 t	µs
t_{WD}	1.0 t	µs
t_{DW}	4.0 t	µs
t_{AW}	6.0 t	µs

Instruction fetch from external program memory

t_{AL}	0.5 t	µs
t_{CA}	5.0 t	µs
t_{LA}	–	µs
t_{CC}	1.0 t	µs
t_{DR}	–	µs
t_{RD}	0.5 t	µs
t_{AD}	1.5 t	µs
t_{ADD}	2.0 t	µs
t_{AFC}	0.5 t	µs

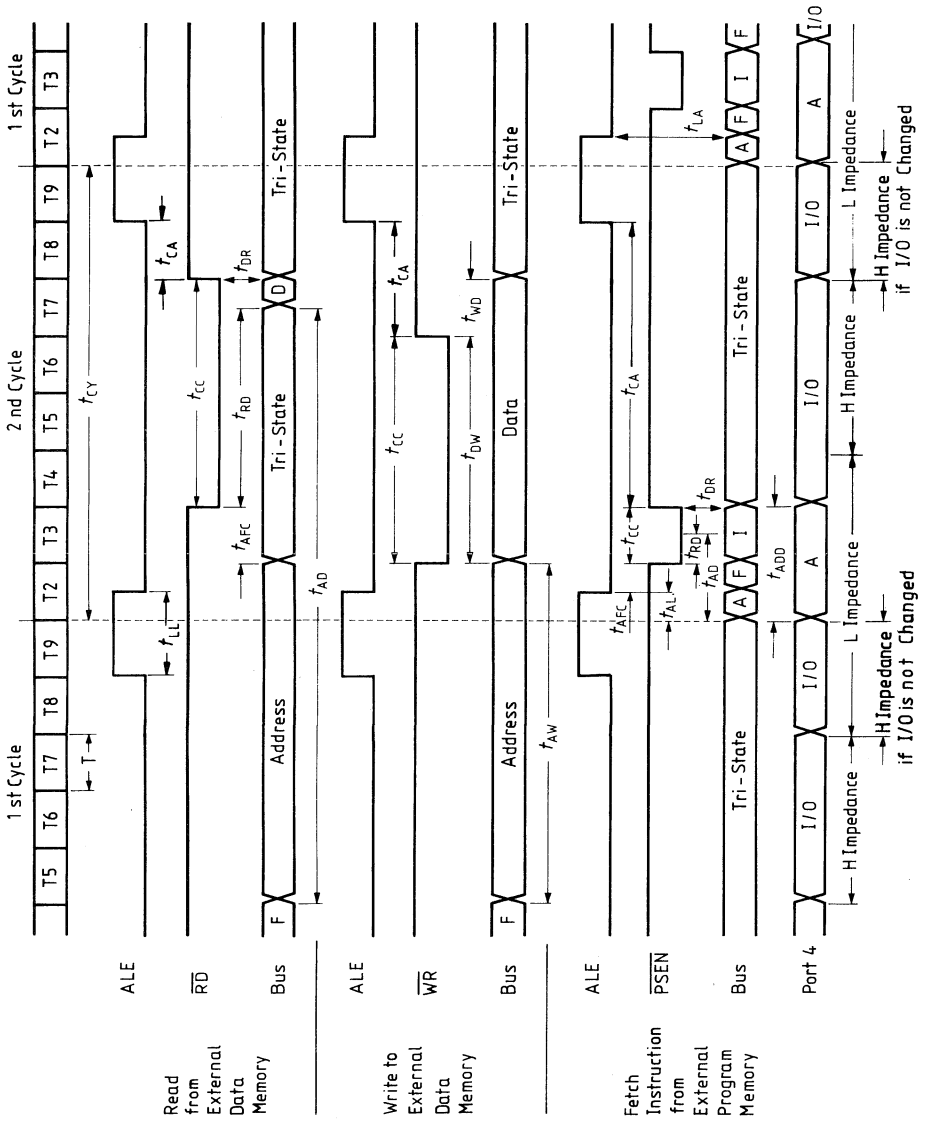
Application Example "Intelligent Telephone Set"



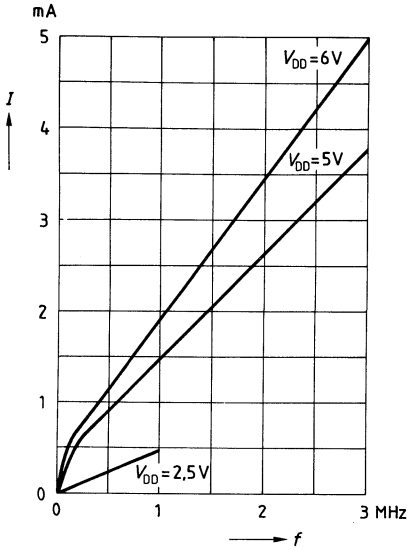
Features of this Telephone set

- direct and indirect redialing
- short dialing (10 memories)
- auto dialing by special keys
- babysitter function
- LC-display control
- electronic keylock
- clock function
- rate signaling

Pulse Diagram SAB 80C482



Max. current consumption versus clock frequency

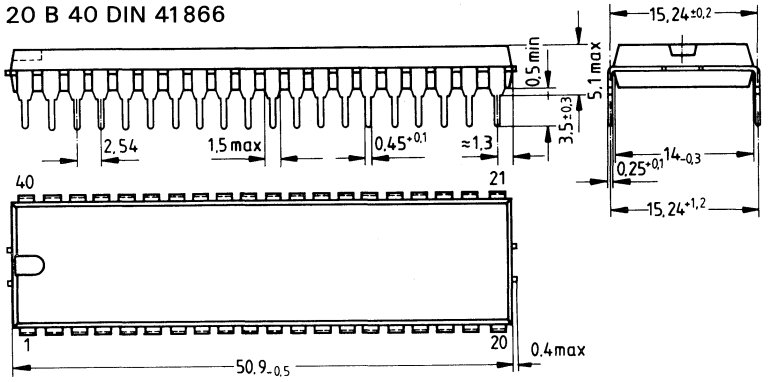


V_{IL} = 0,75 V V_{IH} = 0,7 V_{DD}

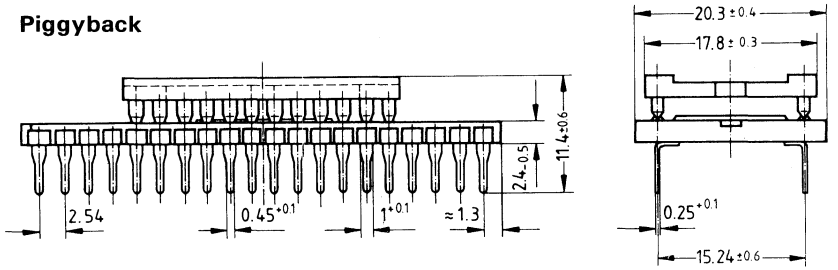
All outputs are not connected

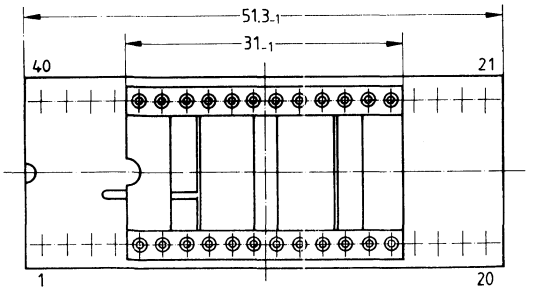
Type	Ordering code	Package
SAB 80C482	Q67100-Z154	P-DIP 40
SAB 80C382	Q67100-H3205	P-DIP 40
SAB 80C382-PC	Q67100-H3199	Piggyback
SAB 80C382-MP	Q67100-H3242	MIKROPACK (SMD)
SAB 80C382-W	Q67100-H8300	PLCC 44 (SMD)

Plastic package, P-DIP, 40 pins
20 B 40 DIN 41866



Piggyback

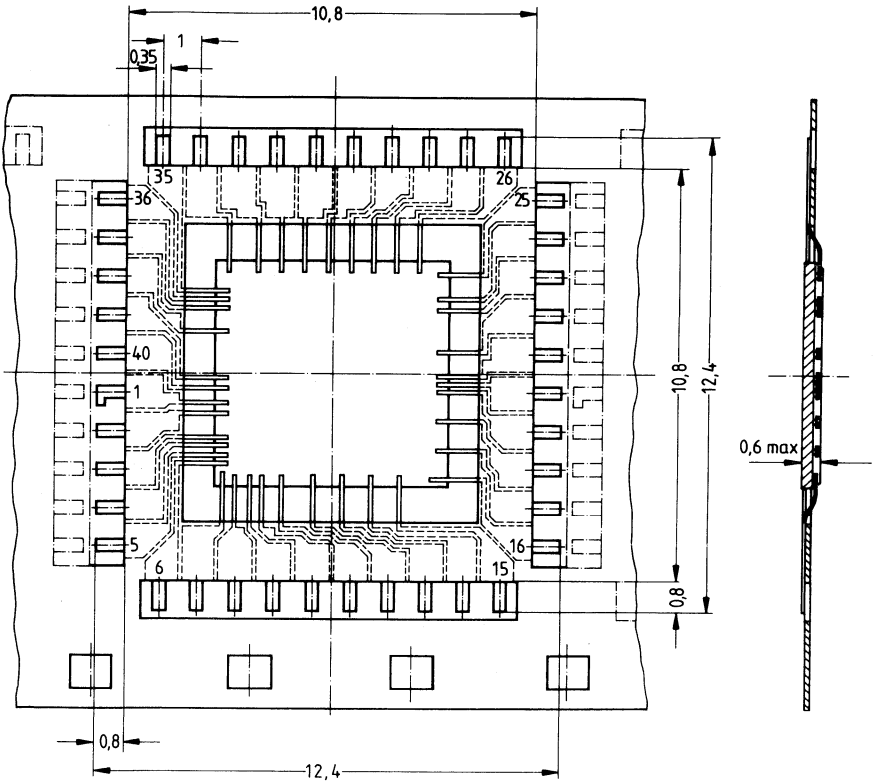




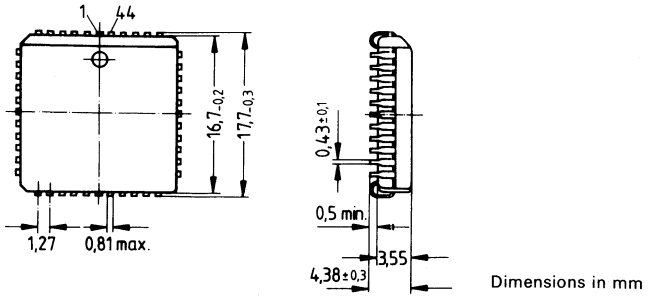
Dimensions in mm

SMD = Surface Mounted Devices

MIKROPACK, 40 pins (SMD)



Plastic package, PLCC, 44 pins (SMD)



Dimensions in mm

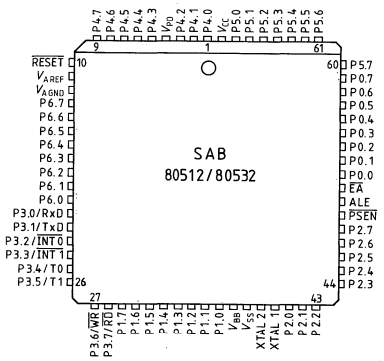
Preliminary

SAB 80512/80532
8-Bit Single-Chip Microcontroller

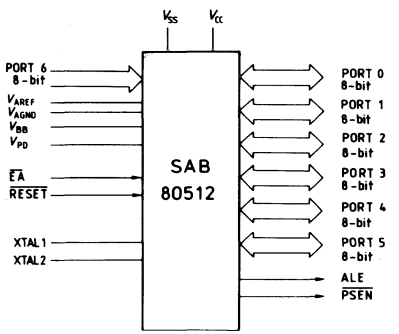
SAB 80512-N	Microcontroller with factory-maskprogrammable ROM
SAB 80532-N	Microcontroller for external ROM
SAB 80512-T40/85-N	Extended temperature range: −40 to +85°C
SAB 80532-T40/85-N	Extended temperature range: −40 to +85°C

- 4K × 8 ROM (SAB 80512 only)
- 128 × 8 RAM
- Full backward compatibility to SAB 8051A/8031A
- Seven 8-bit ports
- Two 16-bit timers/event counters
- High performance full duplex serial channel with own baud rate generator
- 8-bit A/D converter with eight multiplexed inputs, reference voltages externally adjustable
- Six interrupt sources (2 external, 4 internal), two priority levels programmable
- Boolean processor
- 1 µs instruction cycle time (at 12 MHz osc. frequency)
- 4µs multiply and divide (at 12 MHz osc. frequency)
- External program and data memory expandable up to 64 Kbyte each
- PL-CC-68 package

Pin Configurations



Logic Symbol



The SAB 80512/80532 is a new member of the Siemens SAB 8051 family of 8-bit microcontrollers. Maintaining all features of the SAB 8051A/8031A, it is fully backward compatible to the SAB 8051A/8031A. Furthermore the SAB 80512/80532 incorporates several enhancements that significantly increase design flexibility and cost effectiveness. Compared to the SAB 8051A/8031A the SAB 80512/80532 additionally contains an 8-bit A/D converter with 8 multiplexed inputs (these inputs can also be used as digital inputs), an own baud rate generator for the serial interface and two more I/O ports. The SAB 80532 is identical with the SAB 80512, except that it lacks the on-chip ROM.
The SAB 80512/80532 is fabricated in +5V advanced N-channel, silicon gate MYMOS technology of Siemens and supplied in a PL-CC-68 package.
For the industrial temperature range −40 to +85°C, the SAB 80512/80532-T40/85 is available.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
V_{PD}	4	–	Power down supply voltage. If V_{PD} is held within its specifications while V_{CC} drops below the specification, V_{PD} will provide standby power to 40 byte of internal RAM (addr. 58H to 7FH). During normal operation of the SAB 80512, the RAM's current is supplied by V_{CC}, when V_{PD} is low.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80512. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	–	Reference voltage for the A/D converter
V_{AGND}	12	–	Reference ground for the A/D converter
P6.7-P6.0	13-20	I	Port 6, 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages and for the eight multiplexed analog inputs of the A/D converter, simultaneously.
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input / timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

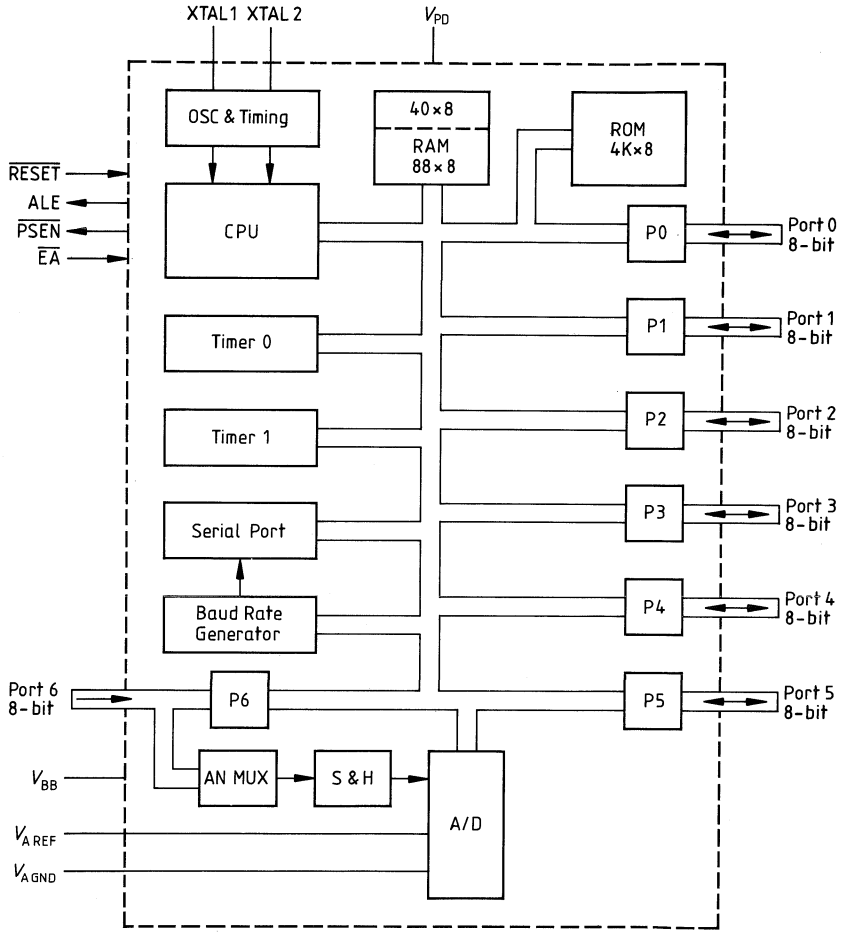
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. The port is also used for the low order address byte during program verification.
V_{BB}	37	–	Substrate pin. Must be connected to V_{SS} with a capacitor (100 nF to 1000 nF) for proper operation of the A/D converter.
XTAL2 XTAL1	39 40	– –	XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed: XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80512 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 80512 fetches all instructions from external program memory. For the SAB 80532 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 5 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
V_{CC}	68	–	Supply voltage during normal operation and program verification.
V_{SS}	38	–	Ground (0V)

Block Diagram



Functional Description

The SAB 80512/80532 is based on the architecture of the SAB 8051 microcontroller familiy. The SAB 80512 includes all features of the SAB 8051 and additionally offers peripheral extensions in three items:
- bit A/D converter with adjustable reference voltages
- two more ports
- dedicated baud rate generator

Different to the SAB 8051 is the inverted reset-input and the RAM power-down supply by a special pin (V_{PD}), which supplies 40 byte with a typical current of 2 mA. Beside the backward compatibility to the SAB 8051 (all SAB 8051 software runs on the SAB 80512 without any changes) the SAB 80512 is also upwardly compatible to the SAB 80515. The SAB 80512 is packed into the PL-CC-68 package and has got the same pinning as the SAB 80515.

A/D Converter

The 8-bit A/D converter of the SAB 80512 has 8 multiplexed analog inputs and uses the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated. The SAB 80512 provides variable external reference voltages V_{AGND} and V_{AREF} adjustable in a wide range. A compressed reference voltage range allows to increase the resolution of the converted analog input. The lower reference voltage (V_{AGND}) can be varied within V_{SS}-0.2V and 4V, the higher (V_{AREF}) within 1V and V_{CC} +5%. For proper operation of the A/D converter a minimum of 1V difference is required between the external voltages:

$(V_{SS}-0.2V) \leq V_{AGND} \leq (V_{AREF}-1V)$

$(V_{AGND}+1V) \leq V_{AREF} \leq (V_{CC}+5\%)$

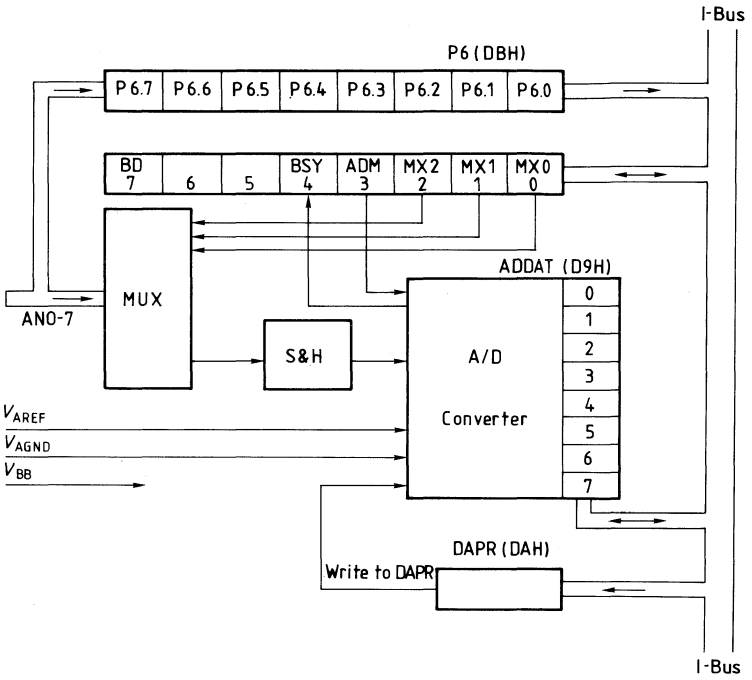
Special Function Register

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 28 special function registers (SFRs) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area.

I/O Ports

The SAB 80512 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, ports 1 to 5 will pull high and will source current when externally pulled low. Port 0 will float when configured as input.
Port 6 is an input port only and can be used as digital input port, if the values meet the specified high/low voltages and as analog input for the A/D-converter.
Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Block Diagram of A/D Converter



Special Function Registers

Address	Symbol	Name	bit-addressable
80H	P0	Port 0 Register	yes
81H	SP	Stack Pointer	–
82H	DPL	Data Pointer, low-byte	–
83H	DPH	Data Pointer, high-byte	–
87H	PCON	Power Control Register	–
88H	TCON	Timer Control Register	yes
89H	TMOD	Timer Mode Register	–
8AH	TL0	Timer 0, low-byte	–
8BH	TL1	Timer 1, low-byte	–
8CH	TH0	Timer 0, high-byte	–
8DH	TH1	Timer 1, high-byte	-
90H	P1	Port 1 Register	yes
98H	SCON	Serial Port Control Register	yes
99H	SBUF	Serial Port Buffer Register	–
0A0H	P2	Port 2 Register	yes
0A8H	IE	Interrupt Enable Register	yes
0B0H	P3	Port 3 Register	yes
0B8H	IP	Interrupt Priority Register	yes
0C0H	IRCON	Interrupt Request Control	yes
0D0H	PSW	Program Status Word Register	yes
0D8H	ADCON	A/D Converter Control Register	yes
0D9H	ADDAT	A/D Converter Data Register	–
0DAH	DAPR	D/A Converter Start Register	–
0DBH	P6	Port 6 Register	–
0E0H	ACC	Accumulator Register	yes
0E8H	P4	Port 4 Register	yes
0F0H	B	B-Register	yes
0F8H	P5	Port 5 Register	yes

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	1
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Data transfer

MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

Boolean variable manipulation

CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn — Working register R0–R7
direct — 128 internal RAM locations, any I/O port, control or status register
@Ri — Indirect internal or external RAM location addressed by register R0 or R1
#data — 8-bit constant included in instruction
#data 16 — 16-bit constant included as bytes 2 and 3 of instruction
bit — 128 software flags, any I/O pin, control or status bit
A — Accumulator

Notes on program addressing modes:

addr 16 — Destination address for LCALL and LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11 — Destination address for ACALL and AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	addr.11
02	3	LJMP	addr.16
03	1	RR	A
04	1	INC	A
05	2	INC	direct
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit,rel*
11	2	ACALL	addr.11
12	3	LCALL	addr.16
13	1	RRC	A
14	1	DEC	A
15	2	DEC	direct
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit,rel*
21	2	AJMP	addr.11
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,direct
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit,rel*
31	2	ACALL	addr.11
32	1	RETI	
33	1	RLC	A

Hex code	Number of bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,direct
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	*rel*
41	2	AJMP	addr.11
42	2	ORL	direct,A
43	3	ORL	direct,#data
44	2	ORL	A,#data
45	2	ORL	A,direct
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*rel*
51	2	ACALL	addr.11
52	2	ANL	direct,A
53	3	ANL	direct,#data
54	2	ANL	A,#data
55	2	ANL	A,direct
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*rel*
61	2	AJMP	addr.11
62	2	XRL	direct,A
63	3	XRL	direct,#data
64	2	XRL	A,#data
65	2	XRL	A,direct
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*rel*
71	2	ACALL	*addr. 11*
72	2	ORL	C,*bit*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*direct*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*rel*
81	2	AJMP	*addr. 11*
82	2	ANL	C,*bit*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*direct,direct*
86	2	MOV	*direct*,@R0
87	2	MOV	*direct*,@R1
88	2	MOV	*direct*,R0
89	2	MOV	*direct*,R1
8A	2	MOV	*direct*,R2
8B	2	MOV	*direct*,R3
8C	2	MOV	*direct*,R4
8D	2	MOV	*direct*,R5
8E	2	MOV	*direct*,R6
8F	2	MOV	*direct*,R7
90	3	MOV	DPTR,#*data 16*
91	2	ACALL	*addr. 11*
92	2	MOV	*bit*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*direct*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,*bit*#
A1	2	AJMP	*addr. 11*
A2	2	MOV	C,*bit*
A3	1	INC	DPTR
A4	1	MUL	AB
A5	2	reserved	
A6	2	MOV	@R0,*direct*
A7	2	MOV	@R1,*direct*
A8	2	MOV	R0,*direct*
A9	2	MOV	R1,*direct*
AA	2	MOV	R2,*direct*
AB	2	MOV	R3,*direct*
AC	2	MOV	R4,*direct*
AD	2	MOV	R5,*direct*
AE	2	MOV	R6,*direct*
AF	2	MOV	R7,*direct*
B0	2	ANL	C,/*bit*
B1	2	ACALL	*addr. 11*
B2	2	CPL	*bit*
B3	1	CPL	C
B4	3	CJNE	A,#*data,rel*
B5	3	CJNE	A,*direct,rel*
B6	3	CJNE	@R0,#*data,rel*
B7	3	CJNE	@R1,#*data,rel*
B8	3	CJNE	R0,#*data,rel*
B9	3	CJNE	R1,#*data,reel*
BA	3	CJNE	R2,#*data,rel*
BB	3	CJNE	R3,#*data,rel*
BC	3	CJNE	R4,#*data,rel*
BD	3	CJNE	R5,#*data,rel*
BE	3	CJNE	R6,#*data,rel*
BF	3	CJNE	R7,#*data,rel*
C0	2	PUSH	*direct*
C1	2	AJMP	*addr. 11*
C2	2	CLR	*bit*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*direct*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*direct*
D1	2	ACALL	*addr. 11*
D2	2	SETB	*bit*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*direct, rel*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*rel*
D9	2	DJNZ	R1,*rel*
DA	2	DJNZ	R2,*rel*
DB	2	DJNZ	R3,*rel*
DC	2	DJNZ	R4,*rel*
DD	2	DJNZ	R5,*rel*
DE	2	DJNZ	R6,*rel*
DF	2	DJNZ	R7,*rel*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*addr. 11*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*direct* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*addr. 11*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*direct,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Temperature under bias	0 to + 70°C for the SAB 80512/80532
	−40 to + 85°C for the SAB 80512/80532-T40/85
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$;
$T_A = 0$ to 70°C; for SAB 80512/80532
$T_A = -40$ to +85°C for SAB 80512/80532-T40/85

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{RESET}$ and XTAL2)	2.0	V_{CC}+0,5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC}+0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{RESET}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	$I_{OL} = 1.6$ mA
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$	–	0.45	V	$I_{OL} = 3.2$ mA
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	$I_{IOH} = -80\,\mu A$
V_{OH1}	Output high voltage, port 0, ALE, $\overline{PSEN}$	2.4	–	V	$I_{OH} = -400\,\mu A$
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	−500	µA	$V_{IL} = 0.45$ V
I_{IL2}	Logic 0 input current, XTAL2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45$ V
I_{IL3}	Input low current to $\overline{RESET}$ for reset	–	−500	µA	$V_{IL} = 0.45\,V$
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	$0\,V < V_{IN} < V_{CC}$
I_{CC}	Power supply current SAB 80512/80532 SAB 80512/80532-T40/85	–	175	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	$V_{CC} = 0\,V$
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1$ MHz

A/D Converter Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V;
(V_{SS} −0.2 V) ≤ V_{AGND} ≤ (V_{AREF} −1V); (V_{AGND}+1V) ≤ V_{AREF} ≤ (V_{CC}+ 5%);
T_A = 0 to 70°C for SAB 80512/80532
T_A = −40 to +85°C for SAB 80512/80532-T40/85

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND} −0.2	–	V_{AREF} +0.2	V	–
C_I	Analog input capacitance	–	25	70	pF	[1]
t_L	Load time	–	–	2 t_{CY}	µs	
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	µs	
t_C	Conversion time (incl. sample time)	–	–	15 t_{CY}	µs	
DNLE	Differential non-linearity	–	±1/2	±1	LSB	$V_{AREF} = V_{CC}$ $V_{AGND} = V_{SS}$
INLE	Integral non-linearity	–	±1/2	±1		
	Offset error	–	±1/2	±1		
	Gain error	–	±1/2	±1		
TUE	Total unadjusted error	–	±1	±2		[1] [2]
I_{REF}	V_{AREF} supply current	–	–	5	mA	[2]

[1] The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

[2] The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$
$T_A = 0$ to 70°C for SAB 80512/80532
$T_A = -40$ to +85°C for SAB 80512/80532-T40/85
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	Address to valid instr in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instr in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instr in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

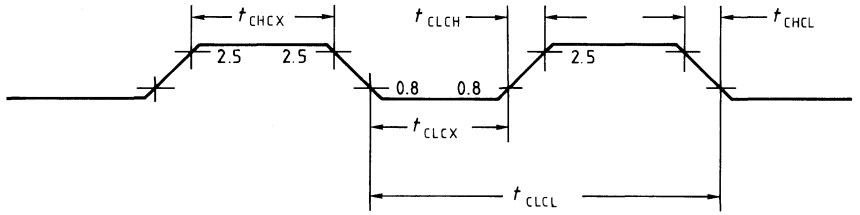
Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{TCLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132		$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	250	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 80512 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

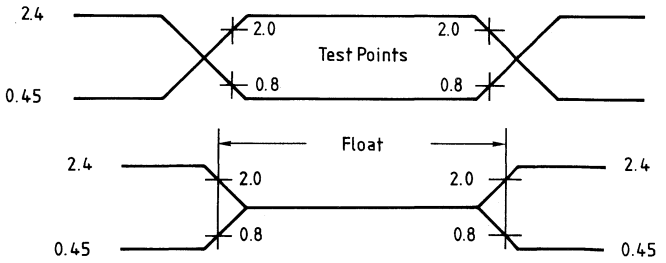
External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCK}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



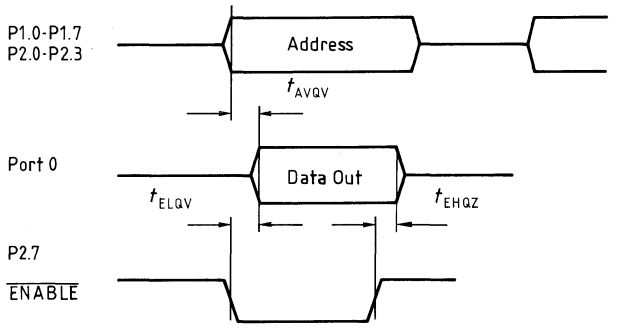
AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



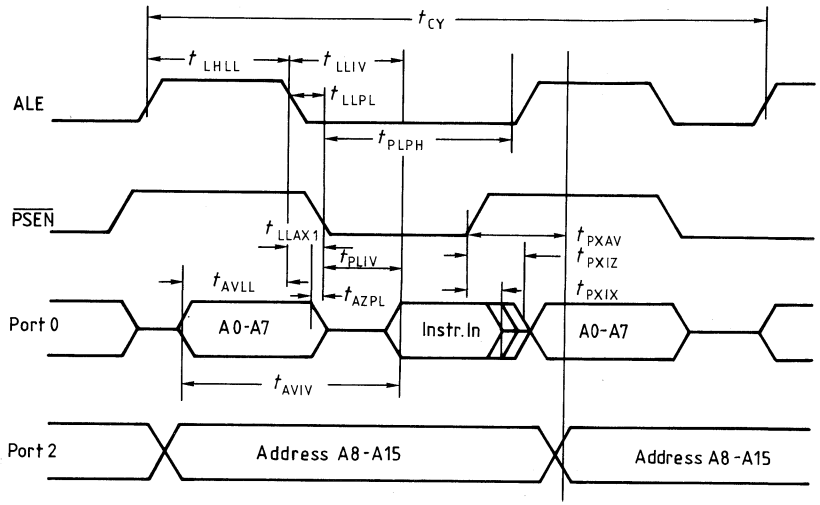
Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11

Data: Port 0 = D0–D7

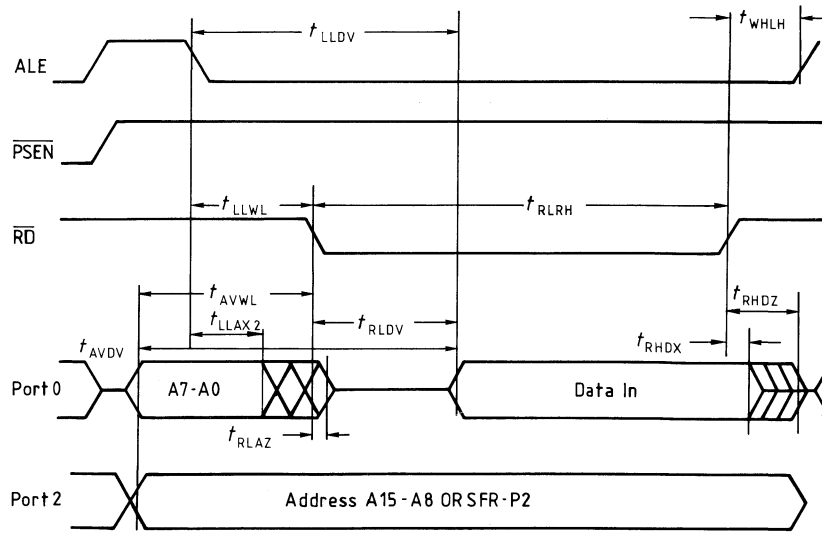
Inputs: P2.4–P2.6, $\overline{PSEN} = V_{SS}$
$\overline{ALE}$, $\overline{EA} = V_{IH}$
$\overline{RESET} = V_{IL}$

Waveforms

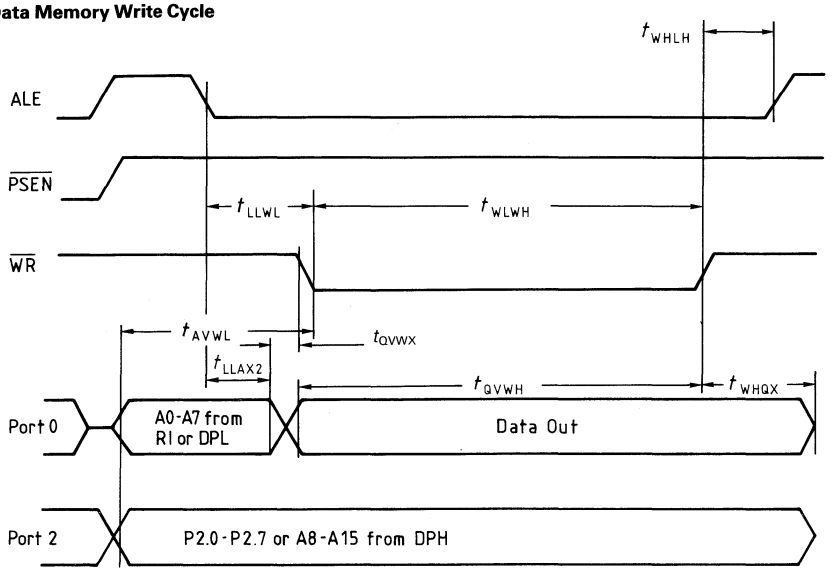
Program Memory Read Cycle



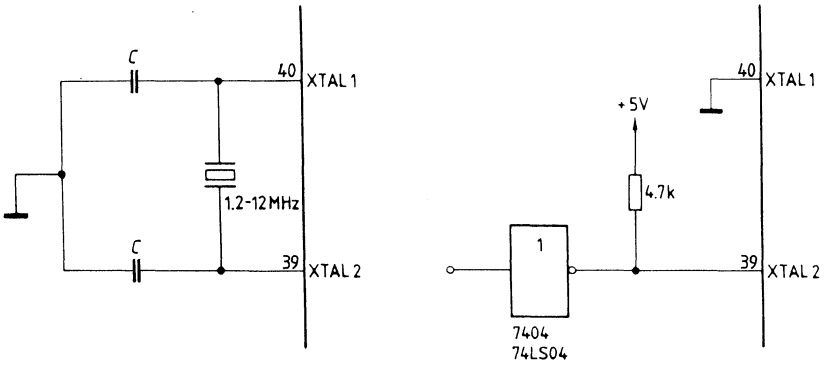
Data Memory Read Cycle



Data Memory Write Cycle



Recommended Oscillator Circuits



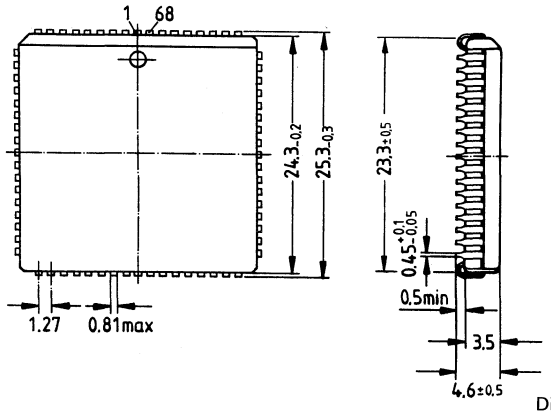
$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

Driving from External Source

Package Outlines

68-Pin Plastic Leaded Chip Carrier Package, PL-CC-68 (SMD)



Dimensions in mm

Ordering Information

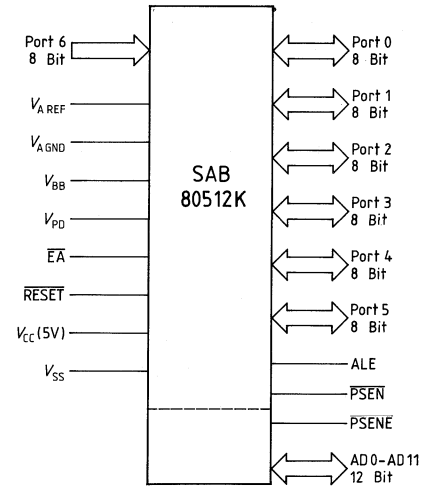
Type	Ordering code	Function
SAB 80512-N	Q67120-C336	8-bit single-chip microcontroller with ROM
SAB 80532-N	Q67120-C337	8-bit single-chip microcontroller for external ROM
SAB 80512-T40/85-N	Q67120-C353	like SAB 80512 but for −40 to +85°C
SAB 80532-T40/85-N	Q67120-C354	like SAB 80532 but for −40 to +85°C

Preliminary

SAB 80512K
8-Bit Single-Chip Microcontroller
ROM-less Version

- Additional bus interface for external memory
- 128 × 8 RAM
- Full upward compatibility to SAB 8051A/8031A
- Seven 8-bit ports
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel with dedicated baud rate generator
- Six interrupt sources (2 external, 4 internal), two priority levels programmable
- 8-bit A/D converter with eight multiplexed inputs, reference voltages externally adjustable
- Boolean processor
- 1 µs instruction cycle time (at 12 MHz oscillator frequency)
- 4 µs multiply and divide (at 12 MHz oscillator frequency)
- External program and data memory expandable to 64 Kbyte each
- Pin grid array package, 88 pins (C-PGA-88)

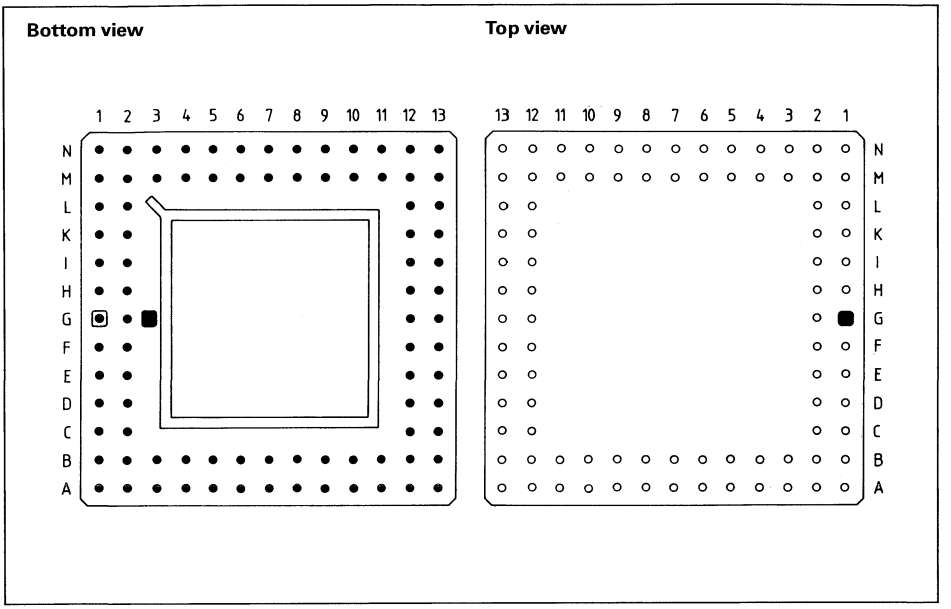
Logic Symbol



The SAB 80512K is a ROM-less version of the 8-bit microcontroller SAB 80512. It contains an additional bus interface to connect an external program memory in place of the SAB 80512's on-chip ROM. Thereby, the SAB 80512K maintains the full I/O capability of the single-chip SAB 80512 while it permits connection of an external memory. All other features of the SAB 80512K are identical with the SAB 80512.

The SAB 80512K is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology, and supplied as pin grid array with 88 pins (C-PGA-88).

Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11	J 13 J 12 K 13 K 12 L 13 M 13 L 12 N 13 N 8 M 7 N 7 M 6	I/O	Multiplexed address/data bus for the program memory. This bus is used for connecting an external memory in place of the 4 Kbyte internal ROM of the SAB 80512. Pins AD0 to AD11 can sink/source 5 LS-TTL loads.
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	N 1 M 2 L 2 M 1 K 2 L 1 K 1 J 2	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have ones written to them are floating, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1 s.
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	F 13 F 12 E 13 E 12 D 13 C 13 D 12 B 13	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	M 11 N 12 M 10 N 11 N 10 M 9 N 9 M 8	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit address (MOVX@DPTR). In this application, port 2 employs strong internal pullup resistors when issuing 1 s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
P3.0 P3.1 P3.2 P3.3 P3.4 P3.5 P3.6 P3.7	A 9 B 9 A 10 B 10 A 11 A 12 B 12 C 12	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0
P4.0 P4.1 P4.2 P4.3 P4.4 P4.5 P4.6 P4.7	D 1 D 2 C 1 C 2 A 1 B 2 B 3 A 2	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.

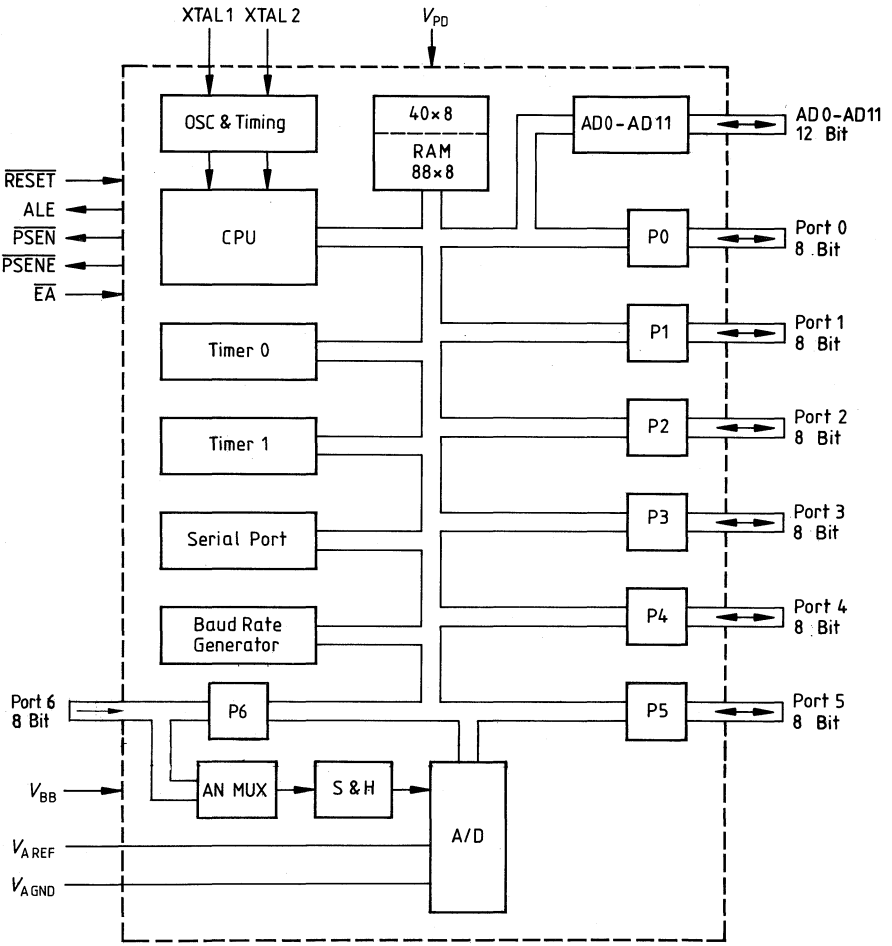
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P5.0 P5.1 P5.2 P5.3 P5.4 P5.5 P5.6 P5.7	E 1 F 1 F 2 G 1 G 2 H 1 H 2 J 1	I/O	Port 5 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.
P6.0 P6.1 P6.2 P6.3 P6.4 P6.5 P6.6 P6.7	A 8 B 8 A 7 B 7 A 6 B 6 A 5 B 5	I	Port 6, 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages and for the eight multiplexed analog inputs of the A/D converter, simultaneously.
XTAL2 XTAL1	H 12 H 13		XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flipflop. Minimum and maximum high and low times specified in the AC characteristics must be observed. XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{RESET}}$	B 4	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80512K. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
ALE	N 2	O	Provides address latch enable output used for latching the address into external memory and emulation memory. It is activated every six oscillator periods except during external data memory accesses.
$\overline{\text{PSEN}}$	N 3	O	The program store enable output is a control signal that enables an external program memory to the bus (port 0 and port 2) during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during program execution from emulation memory.
$\overline{\text{PSENE}}$	M 12	O	This output is a control signal that enables an external program memory to AD0 to AD7 during instruction fetch operations. It is activated every six oscillator periods.
$\overline{\text{EA}}$	M 3	I	When $\overline{\text{EA}}$ is held at a TTL high level, the SAB 80512K executes instructions from the program memory connected to the AD lines when the PC is less than 4096. When $\overline{\text{EA}}$ is held at a TTL low level, the SAB 80512K executes all instructions from external program memory (through port 0 lines).
V_{AREF}	A 3		Reference voltage for the A/D converter
V_{AGND}	A 4		Reference ground for the A/D converter
V_{CC}	E 2		POWER SUPPLY
V_{SS}	G 13		GROUND (0 V)
V_{PD}	B 1		POWER DOWN SUPPLY VOLTAGE If V_{PD} is held within its specifications while V_{CC} drops below the specification, V_{PD} will provide standby power to 40 byte of internal RAM (addresses 58H to 7FH). During normal operation of the SAB 80512K, the RAM's current is supplied by V_{CC} when V_{PD} is low.
V_{BB}	G 12		SUBSTRATE PIN Must be connected to V_{SS} through a capacitor (100 to 1000 nF) for proper operation of the A/D converter.
NC	A 13 B 11 M 4 M 5 N 4 N 5 N 6		NO CONNECTION

Figure 1
Block Diagram



Functional Description

The members of the SAB 80512 microcontroller family are:

- SAB 80512 with factory mask-programmable 4 Kbyte on-chip ROM
- SAB 80532 ROM-less version of the SAB 80512
- SAB 80512K ROM-less version of the SAB 80512 with additional bus interface

In this data sheet the term "SAB 80512" is used to refer generally to all members of the SAB 80512 family, except where specifically stated otherwise.

The SAB 80512 is based on the architecture of the SAB 8051 microcontroller family. The SAB 80512 includes all features of the SAB 8051 and additionally offers peripheral extensions in three items:

- 8-bit A/D converter with adjustable reference voltages
- two more ports
- dedicated baud rate generator

Different to the SAB 8051 is the inverted reset input and the RAM power-down supply by a special pin (V_{PD}), which supplies 40 byte with a typical current of 2 mA. Beside the upward compatibility to the SAB 8051 (all SAB 8051 software runs on the SAB 80512 without any changes) the SAB 80512 is also downward compatible with the SAB 80515.

The SAB 80512K is a ROM-less version of the SAB 80512. In place of the 4 Kbyte on-chip ROM, there is an additional bus interface for an 4 Kbyte emulation memory which can be connected externally.

Figure 1 shows a block diagram of the SAB 80512K.

Program Memory

The SAB 80512 has 4 Kbyte of on-chip ROM, while the SAB 80532 has no internal ROM. The program memory can be externally expanded up to 64 Kbyte. If the $\overline{EA}$ pin is held high, the SAB 80512 executes out of internal ROM unless the address exceeds 0FFFH. Locations 1000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80512 fetches all instructions from the external program memory. Since the SAB 80532 has no internal ROM, pin $\overline{EA}$ must be tied low when using this device.

The SAB 80512K has the same function as the SAB 80512; the difference is that fetches from the internal ROM are executed from the program memory through the additional bus interface.

A/D Converter

The 8-bit A/D converter of the SAB 80512 has 8 multiplexed analog inputs and is using the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated. The SAB 80512 provides variable external reference voltages V_{AGND} and V_{AREF} adjustable in a wide range. A compressed reference voltage range allows to increase the resolution of the converted analog input.

Figure 2 shows a block diagram of the A/D converter of the SAB 80512.

Figure 2
Block Diagram of A/D Converter

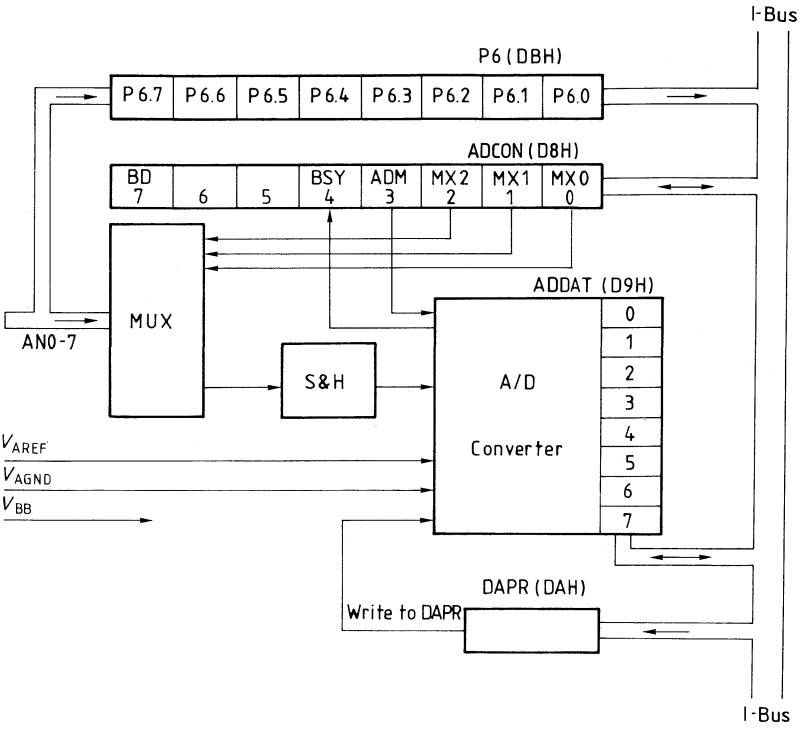


Table 1
Special Function Registers

Address	Symbol	Name	Bit-Addressable
80H	P0	Port 0 register	Yes
81H	SP	Stack pointer	–
82H	DPL	Data pointer, low byte	–
83H	DPH	Data pointer, high byte	–
87H	PCON	Power control register	–
88H	TCON	Timer control register	Yes
89H	TMOD	Timer mode register	–
8AH	TL0	Timer 0, low byte	–
8BH	TL1	Timer 1, low byte	–
8CH	TH0	Timer 0, high byte	–
8DH	TH1	Timer 1, high byte	–
90H	P1	Port 1 register	Yes
98H	SCON	Serial port control register	Yes
99H	SBUF	Serial port buffer register	–
0A0H	P2	Port 2 register	Yes
0A8H	IE	Interrupt enable register	Yes
0B0H	P3	Port 3 register	Yes
0B8H	IP	Interrupt priority register	Yes
0C0H	IRCON	Interrupt request control	Yes
0D0H	PSW	Program status word register	Yes
0D8H	ADCON	A/D converter control register	Yes
0D9H	ADDAT	A/D converter data register	–
0DAH	DAPR	D/A converter start register	–
0DBH	P6	Port 6 register	–
0E0H	ACC	Accumulator register	Yes
0E8H	P4	Port 4 register	Yes
0F0H	B	B register	Yes
0F8H	P5	Port 5 register	Yes

Special Function Registers

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 28 special function registers (SFRs) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1.

I/O Ports

The SAB 80512 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, ports 1 to 5 will pull high and will source current when externally pulled low. Port 0 will float when configured as input.
Port 6 is an input port only and can be used as digital input port, if the values meet the specified high/low voltages and as analog input for the A/D converter.
Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

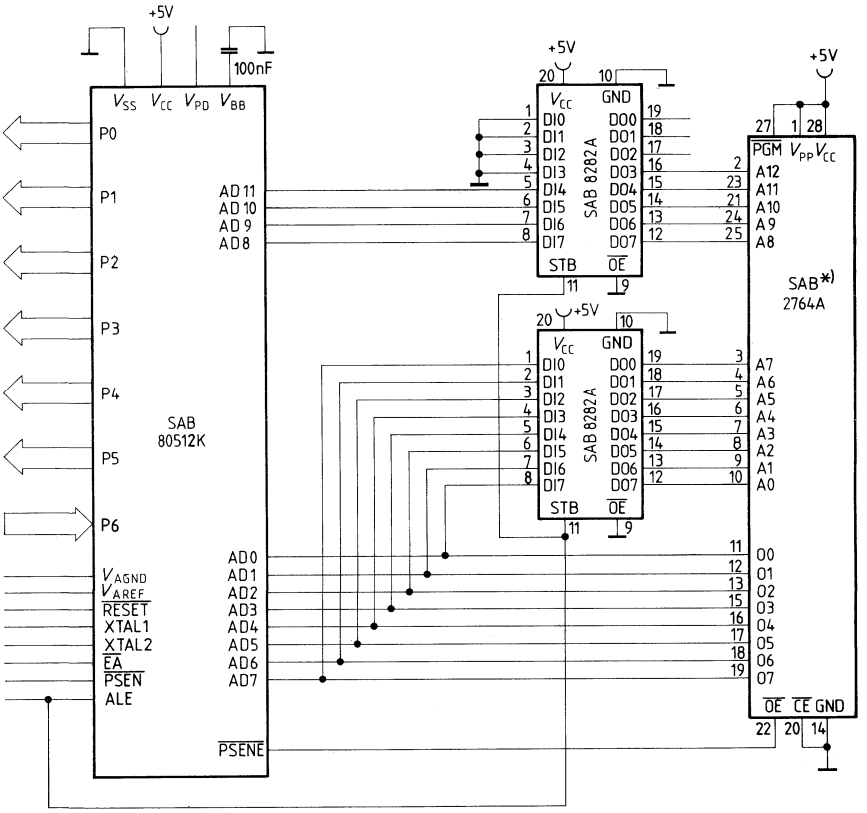
Connecting an External Program Memory to the SAB 80512K

The bond-out chip SAB 80512K allows emulating the SAB 80512's internal ROM via the additional bus interface. The multiplexed bus AD0 to AD1 emits the address and reads the instruction at pins AD0 to AD7. Observe that the higher address lines AD8 to AD11 are also multiplexed. The control signals for the memory connected with AD lines are ALE and $\overline{\text{PSENE}}$.

When pin $\overline{\text{EA}}$ is high, the SAB 80512K executes instructions from the AD bus if the PC is less than 4096, otherwise it will execute from external program memory through P0 and P2. When pin $\overline{\text{EA}}$ is low, the SAB 80512K executes all instructions from external program memory.

Figure 3 shows a typical circuitry to connect a memory to AD0 through AD11 of the SAB 80512K. Although only 4 Kbyte of EPROM are required in this example, the SAB 2764A 8 Kbyte EPROM has been used as it is a standard device. Of course, a 4 Kbyte EPROM like SAB 2732A could also be employed.

Figure 3
Connecting an External Memory to AD0 through AD11



*) Note: Only the lower 4 Kbyte of the SAB 2764A are used

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex code	Number of bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings[1)]

Ambient temperature under bias	0 to + 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

DC Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V; T_A = 0 to 70°C

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{\text{RESET}}$ and XTAL2)	2.0	V_{CC}+0.5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC}+0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{\text{RESET}}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{PSENE}}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OL2}	Output low voltage, AD0 to AD11	–	0.45	V	I_{OL} = 2 mA
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	I_{OH} = −80 µA
V_{OH1}	Output high voltage, port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{PSENE}}$	2.4	–	V	I_{OH} = −400 µA
V_{OH2}	Output high voltage, AD0 to AD11	2.4	–	V	I_{OH} = −2 mA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	−500	µA	V_{IL} = 0.45 V
I_{IL2}	Logic 0 input current, XTAL2	–	−2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IL3}	Input low current to $\overline{\text{RESET}}$ for reset	–	−500	µA	V_{IL} = 0.45 V
I_{LI}	Input leakage current to port 0, $\overline{\text{EA}}$, AD0 to AD11	–	±10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current	–	175	mA	All outputs disconnected
I_{PD}	Power-down current	–	3	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A/D Converter Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$;
$(V_{SS} - 0.2V) \leq V_{AGND} \leq (V_{AREF} - 1V)$; $(V_{AGND} + 1V) \leq V_{AREF} \leq (V_{CC} + 5\%)$

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	$V_{AGND}-$ 0.2	–	$V_{AREF}+$ 0.2	V	–
C_I	Analog input capacitance	–	25	–	pF	[1]
t_S	Sample time	–	–	$5\,t_{CY}$	ns	[1]
t_C	Conversion time (including sample time)	–	–	$15\,t_{CY}$	ns	[1]
	Differential non-linearity	–	±1/2	±1	LSB	$V_{AREF} = V_{CC}$ $V_{AGND} = V_{SS}$ R_I of analog input source ≤10 kΩ
	Integral non-linearity	–	±1/2	±1	LSB	
	Offset error	–	±1/2	±1	LSB	
	Gain error	–	±1/2	±1	LSB	
I_{REF}	V_{AREF} supply current	–	–	5	mA	[2]

[1] The internal resistance of the analog source must be less than 10 kΩ to assure full loading of the sample capacitance during sample time.

[2] The internal resistance of the analog reference voltage source must be less than 1 kΩ.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ±10%; V_{SS} = 0V
(C_L for port 0, ALE, $\overline{PSEN}$ and $\overline{PSENE}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL1}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV1}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL1}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH1}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV1}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX1}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ1} [1]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV1} [1]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV1}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL1}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

[1] Interfacing the SAB 80512K to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

Emulation Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL2}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX3}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV2}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL2}	ALE to $\overline{\text{PSENE}}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH2}	$\overline{\text{PSENE}}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV2}	$\overline{\text{PSENE}}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX2}	Input instruction hold after $\overline{\text{PSENE}}$	0	–	0	–	ns
t_{PXIZ2} [2]	Input instruction float after $\overline{\text{PSENE}}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV2} [2]	Address valid after $\overline{\text{PSENE}}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV2}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL2}	Address float to $\overline{\text{PSENE}}$	0	–	0	–	ns

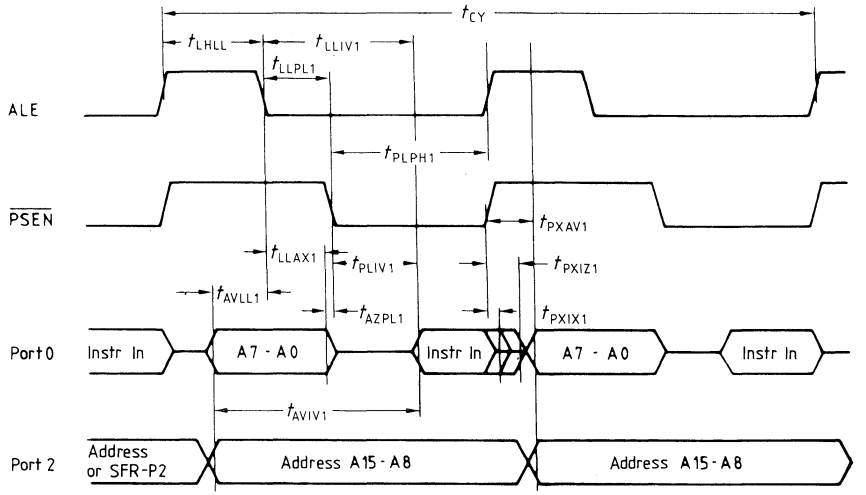
External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCK}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

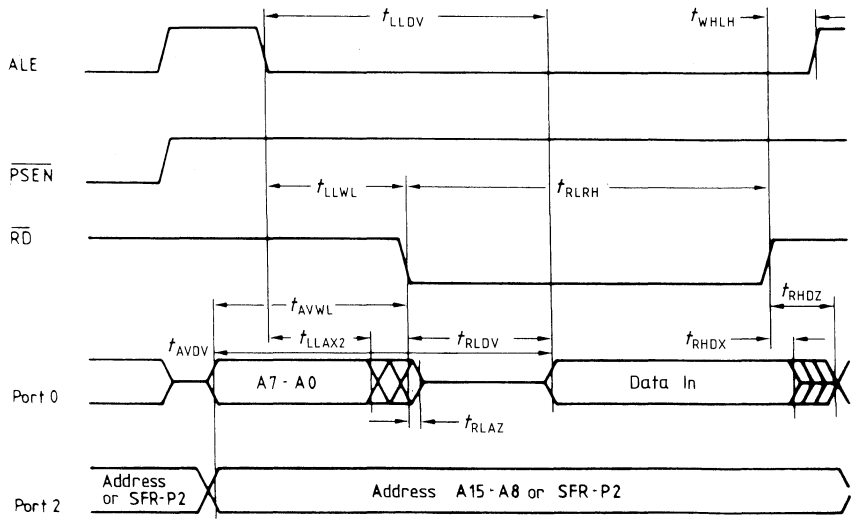
[2] Interfacing the SAB 80512K to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to AD0–AD7 drivers.

Waveforms

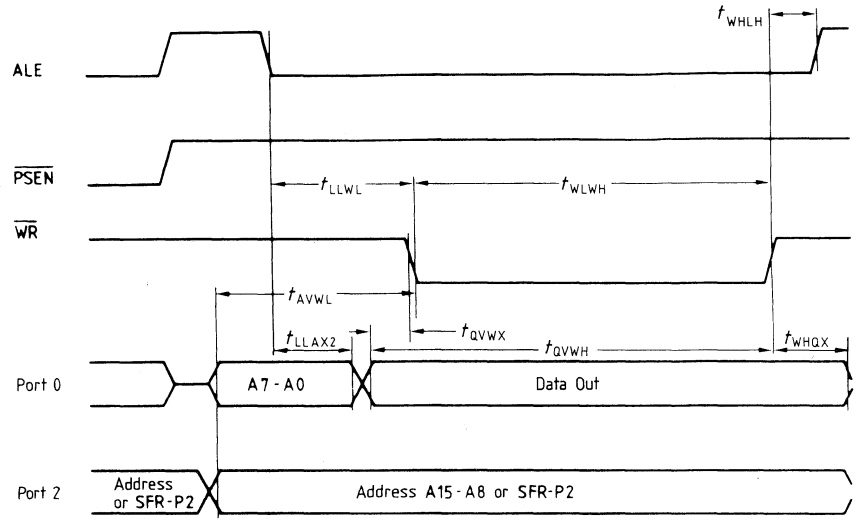
Program Memory Read Cycle



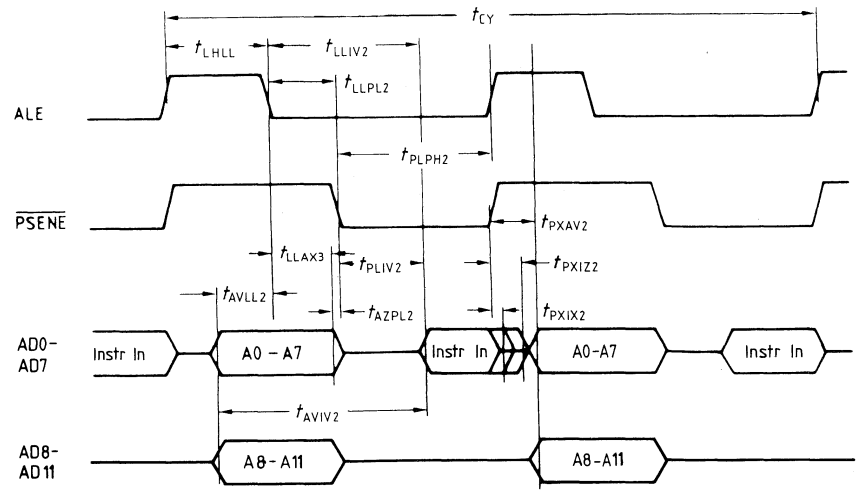
Data Memory Read Cycle



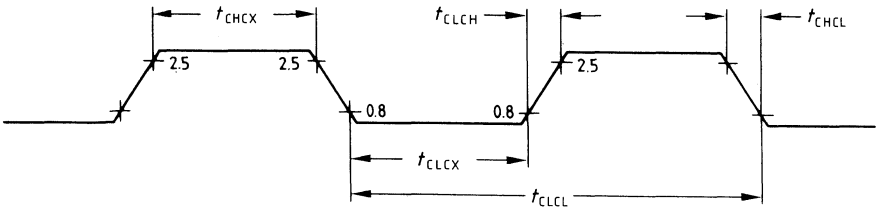
Data Memory Write Cycle



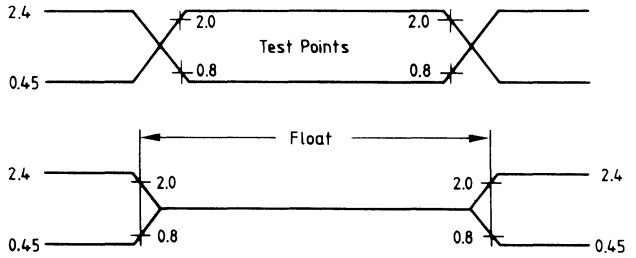
Emulation Memory Read Cycle



External Clock Cycle

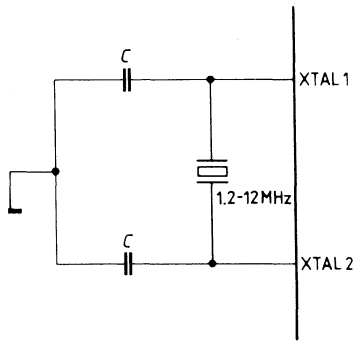


AC Testing Input, Output, Float Waveforms



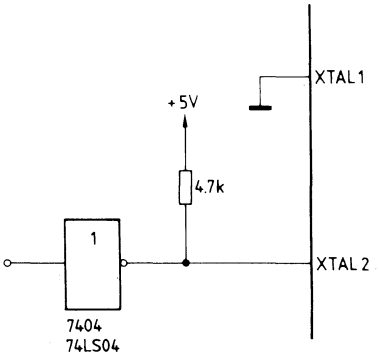
AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pins sinks 3.2 mA or sources 400 µA at voltage test levels.

Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

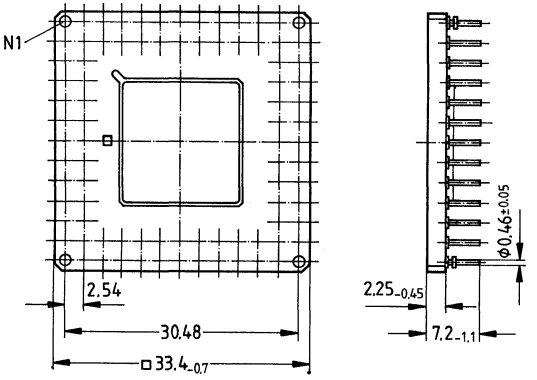
Crystal Oscillator Mode



Driving from External Source

Package Outlines

Ceramic Package, Pin Grid Array, C-PGA-88



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 80512K-A	Q67120-C333	8-bit single-chip microcontroller, ROM-less version

Preliminary

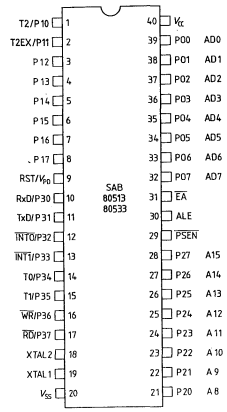
SAB 80513/80533
8-Bit Single-Chip Microcontroller

SAB 80513 Microcontroller with factory-maskprogrammable ROM
SAB 80533 Microcontroller for external ROM

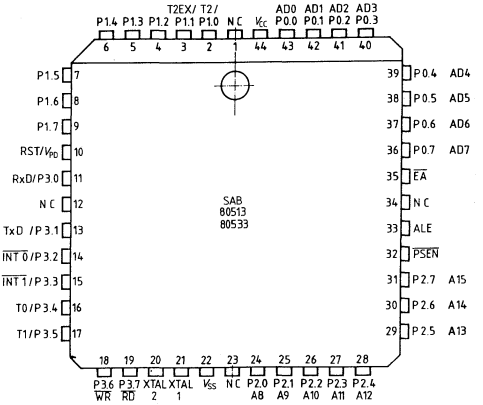
- 16K × 8 ROM (SAB 80513 only)
- 256 × 8 RAM
- Four 8-bit I/O ports
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- Six interrupt vectors, two priority levels are programmable
- Boolean processor
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Fully backward compatible to SAB 8051A and SAB 8052A
- P-DIP 40 and PLCC 44 package

Pin Configuration

P-DIP-40



PLCC 44



The SAB 80513/80533 is a new member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in N-channel, silicon-gate Siemens MYMOS technology.

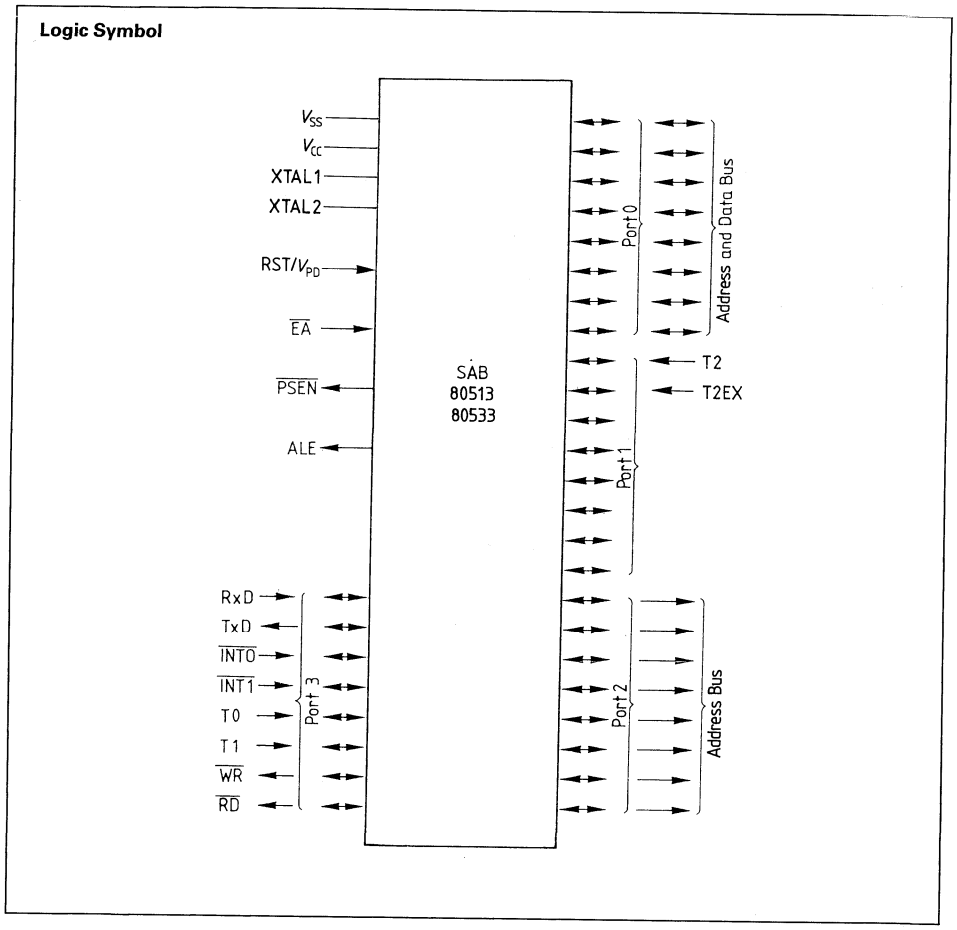
The SAB 80513/80533 is a stand-alone, high-performance, single-chip microcontroller based on the SAB 8051 architecture. It maintains all features of the SAB 8051A and SAB 8052A (including timer 2 of the SAB 8052A) and is thus fully compatible to both the SAB 8051A and SAB 8052A.

In addition, the SAB 80513 contains 16 Kbyte of on-chip ROM, which makes it a powerful and cost-effective controller for applications requiring more ROM space.

Furthermore, the SAB 80513/80533 contains 256 byte RAM on-chip, four 8-bit ports, a powerful interrupt structure with six vectors and two programmable priority levels, a serial channel as well as on-chip oscillator and clock circuitry. The SAB 80533 is identical with the SAB 80513 except that it lacks the on-chip program memory.

The SAB 80513/80533 is supplied in a 40-pin dual-in-line package or a 44-pin plastic leaded chip carrier (PLCC 44) package.

Logic Symbol



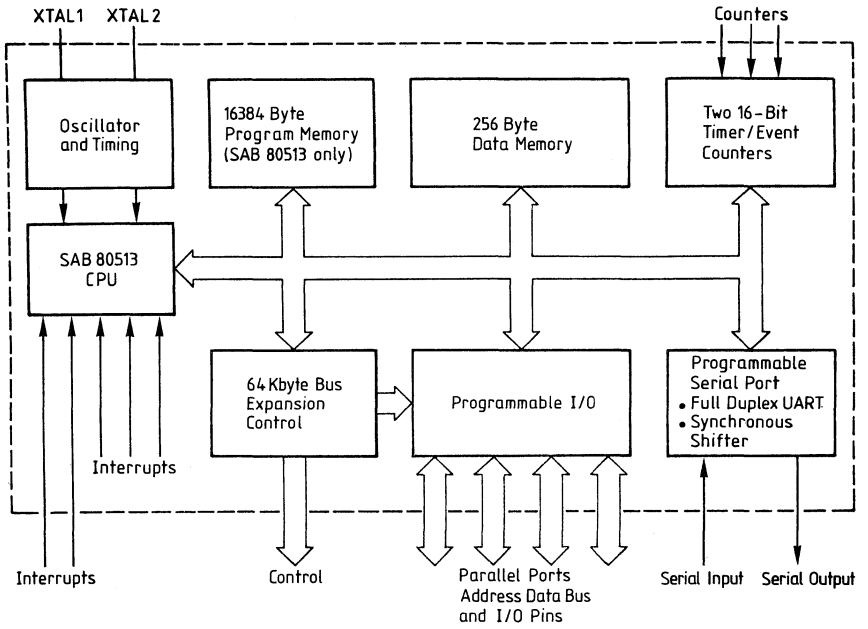
Pin Definitions and Functions

Symbol	Pin P-DIP-40	Pin PLCC 44	Input (I) Output (O)	Function
P1.0–P1.7	1–8	2–9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to timer 2, and T2EX, timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 80513/80533. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20	– 	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	24–31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	PLCC 44		
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an ecternal data memory access.
$\overline{EA}$	31	35	I	When held at a TTL high level, the SAB 80513 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 80513 fetches all instructions from external program memory. For the SAB 80533 this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	Power supply during operation and program verification.
V_{SS}	20	22	–	Ground (0 V)
NC	–	1, 12 23, 34	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/VPD and XTAL2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = −80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = −400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	−500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	−2.0	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/VPD for reset	–	500	µA	V_{IN} = V_{CC} − 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 80513/80533	–	175	mA	All outputs disconnected
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics for SAB 80513/80533

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2\,t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4\,t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3\,t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3\,t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} [1]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} [1]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5\,t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6\,t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6\,t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2\,t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5\,t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2\,t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4\,t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7\,t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

[1]) Interfacing the SAB 80513/80533 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Clock Drive XTAL2

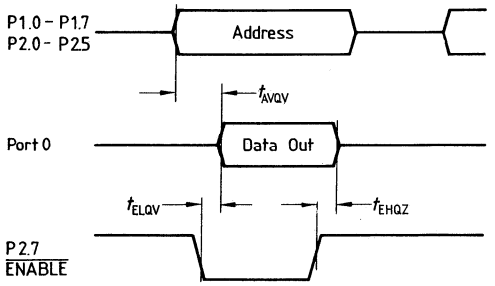
Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

ROM Verification Characteristics for SAB 80513

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

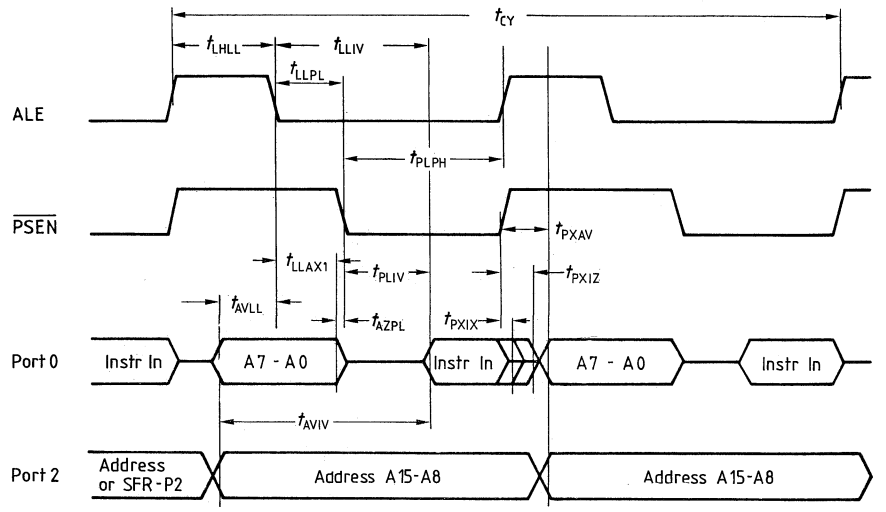


Address: P1.0–P1.7 = A0–A7
P2.0–P2.5 = A8–A13
Data: Port 0 = D0–D7

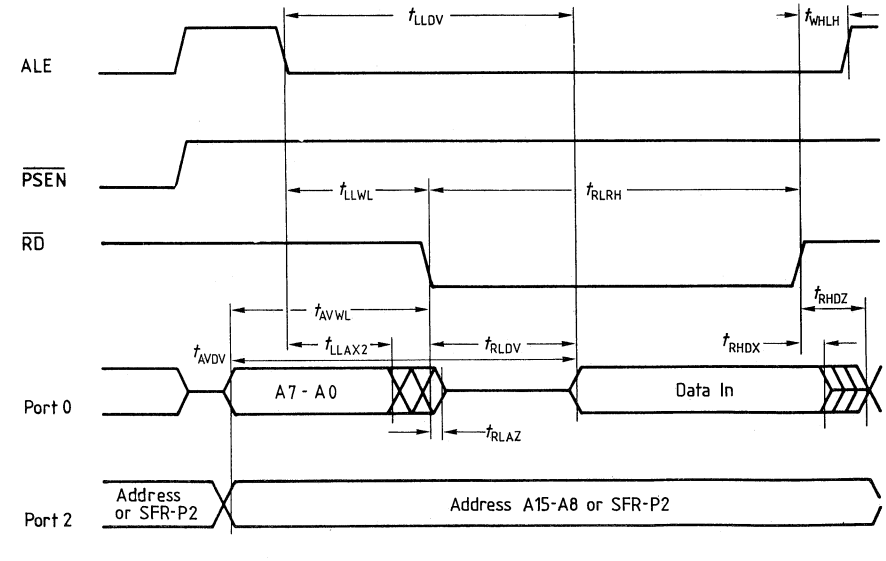
Inputs: P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = V_{IH}
RST/V_{PD} = V_{IH1}

Waveforms

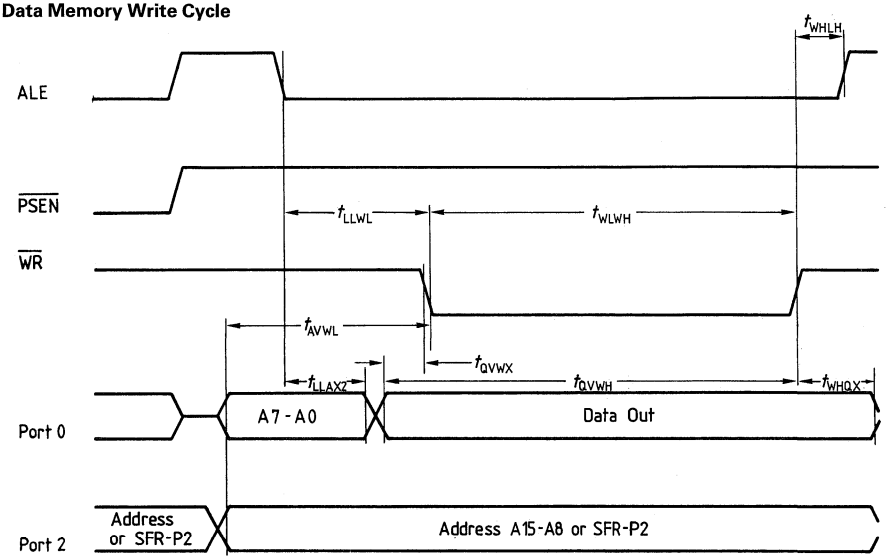
Program Memory Read Cycle



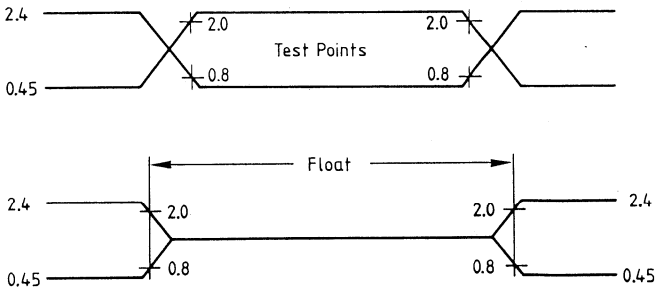
Data Memory Read Cycle



Data Memory Write Cycle

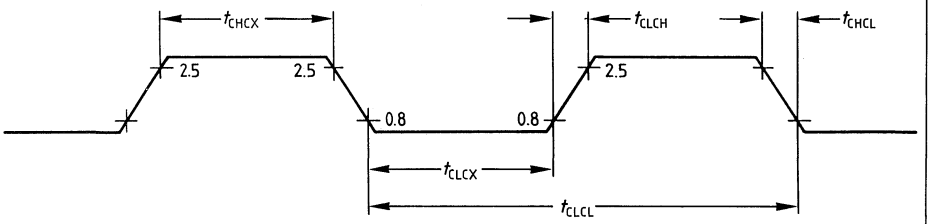


AC Testing Input, Output, Float Waveforms

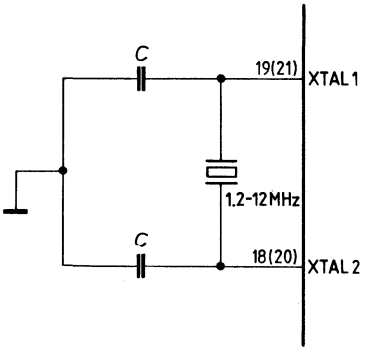


AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

External Clock Cycle

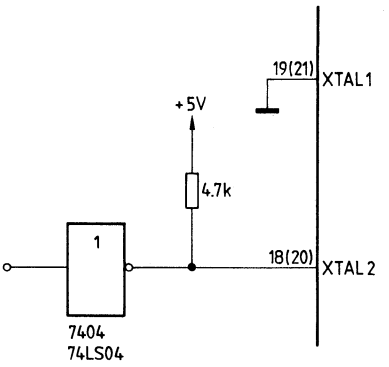


Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

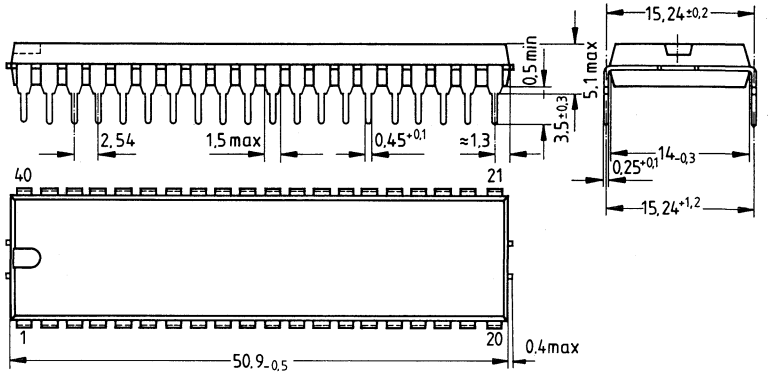


Driving from External Source

Pin numbers in (...) are for PL-CC-44 package

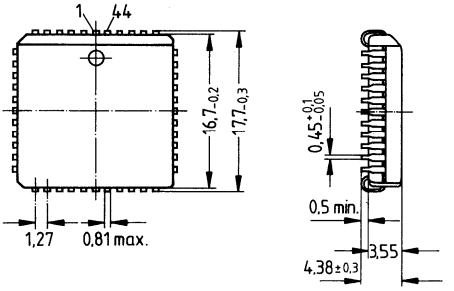
Package Outlines

Plastic Package, P-DIP-40



Dimensions in mm

Plastic Package, PLCC-44



Dimensions in mm

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcontroller
SAB 80513-P	Q 67120-C383	with mask-programmable ROM (P-DIP-40)
SAB 80533-P	Q 67120-C385	for external ROM (P-DIP-40)
SAB 80513-N	Q 67120-C384	with mask-programmable ROM (PLCC-44)
SAB 80533-N	Q 67120-C386	for external ROM (PLCC-44)

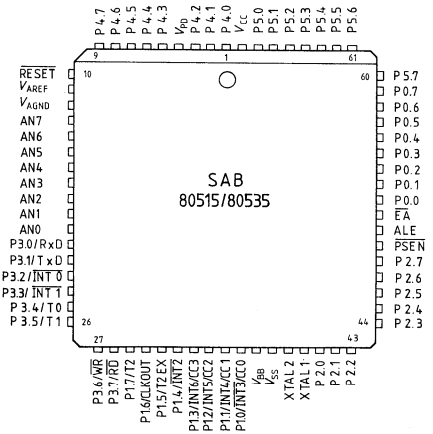
Preliminary

SAB 80515/80535
8-Bit Single-Chip Microcontroller

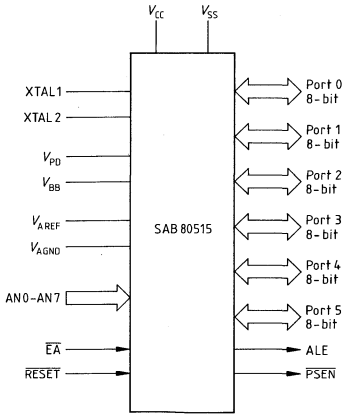
SAB 80515-N **Microcontroller with factory mask-programmable ROM**
SAB 80535-N **Microcontroller for external ROM**

- 8K × 8 ROM (SAB 80515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with eight multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Backwardly compatible with SAB 8051
- 68-pin plastic leaded chip carrier package (PLCC 68)

Pin Configuration (PLCC 68)



Logic Symbol



The SAB 80515/80535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in +5V N-channel, silicon-gate Siemens MYMOS technology.
The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory.
The SAB 80515/80535 is supplied in a 68-pin plastic leaded chip carrier package (PLCC 68).

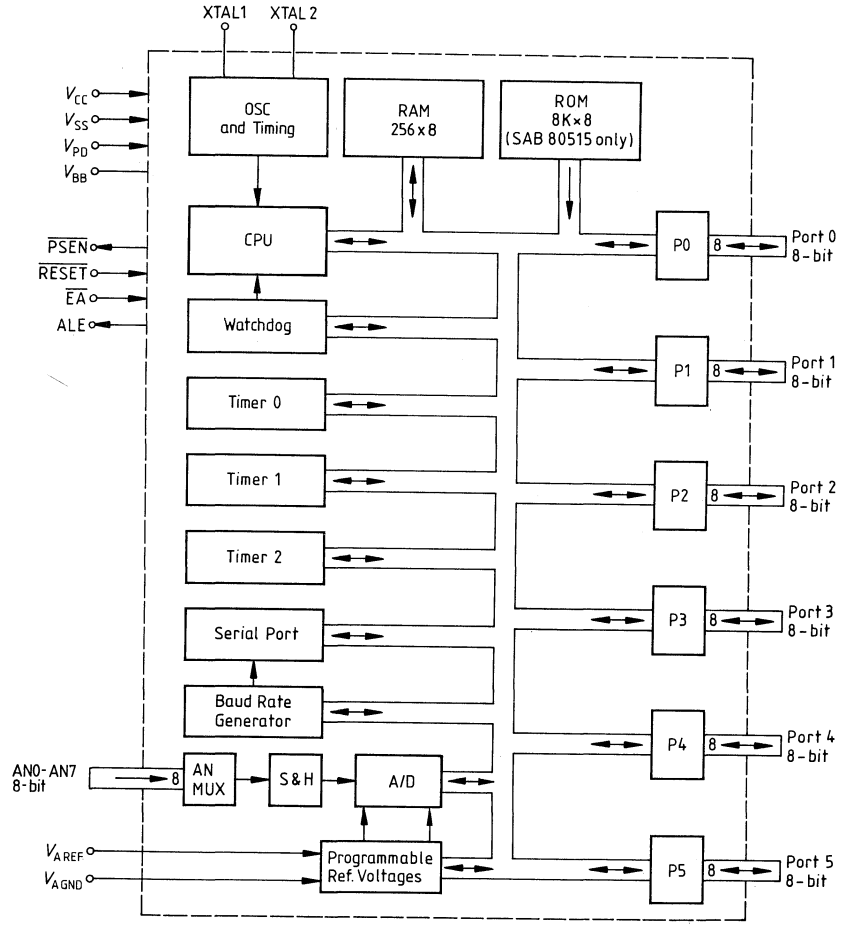
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4		Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0 (cont'd)			– $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39		XTAL2 is the output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40		XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+5V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0V)

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via this interface substitutes the SAB 80515's internal ROM.

The SAB 80535 is identical to the SAB 80515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80515" is used to refer to both the SAB 80515 and SAB 80535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described below:
(Figure 2 illustrates the memory address spaces of the SAB 80515).

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external programm memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

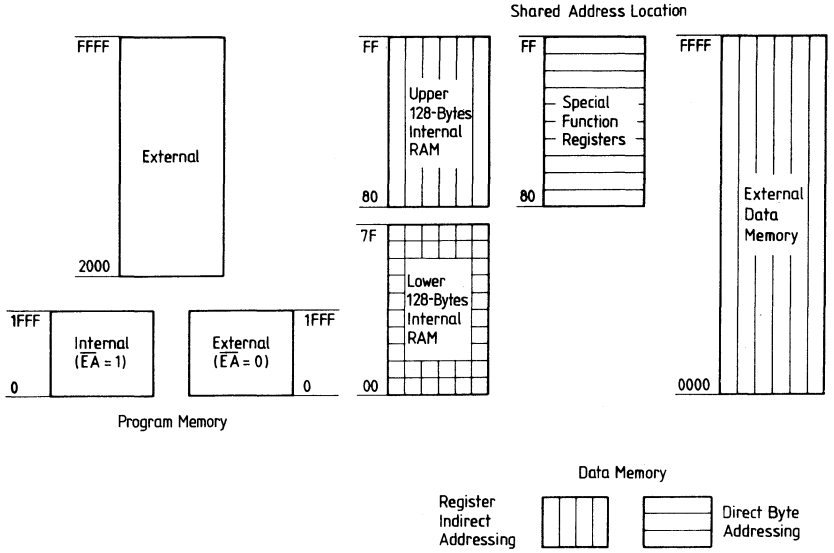
The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D-converter control register	0D8H
ADDAT	A/D-converter data register	0D9H
DAPR	D/A-converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0–AN7 is used for analog input signals to the A/D converter.

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 3 shows a block diagram of the timer/counter 2.

– Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

– Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

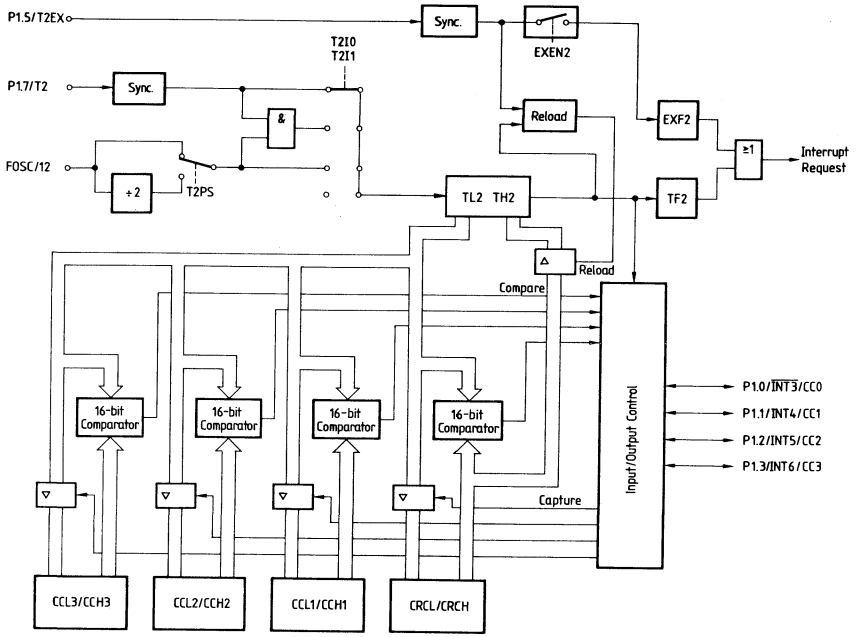
– Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

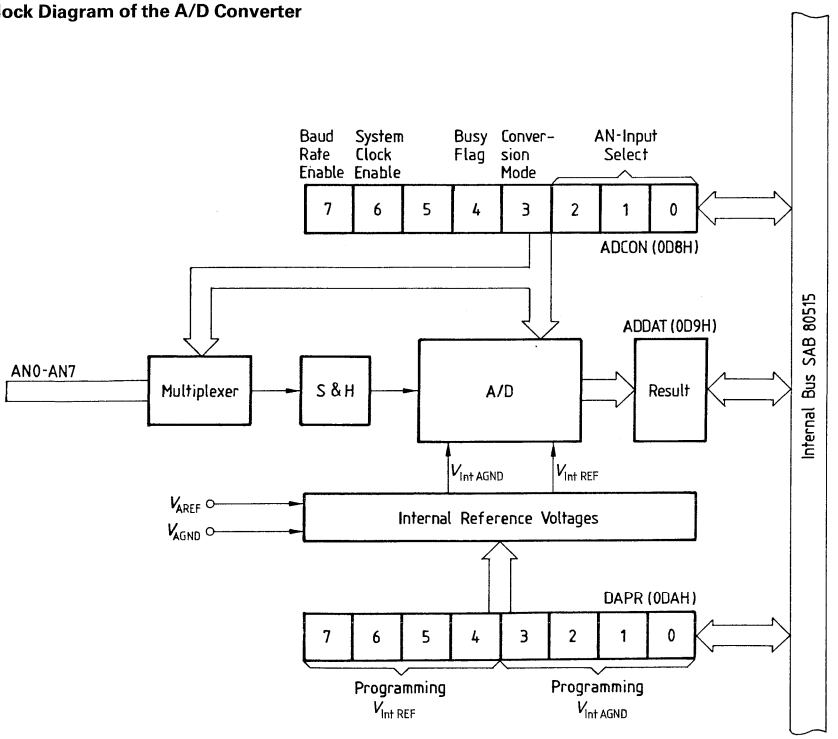
A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 14 machine cycles (14 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (request flags)	Vector	Vector address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/ disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

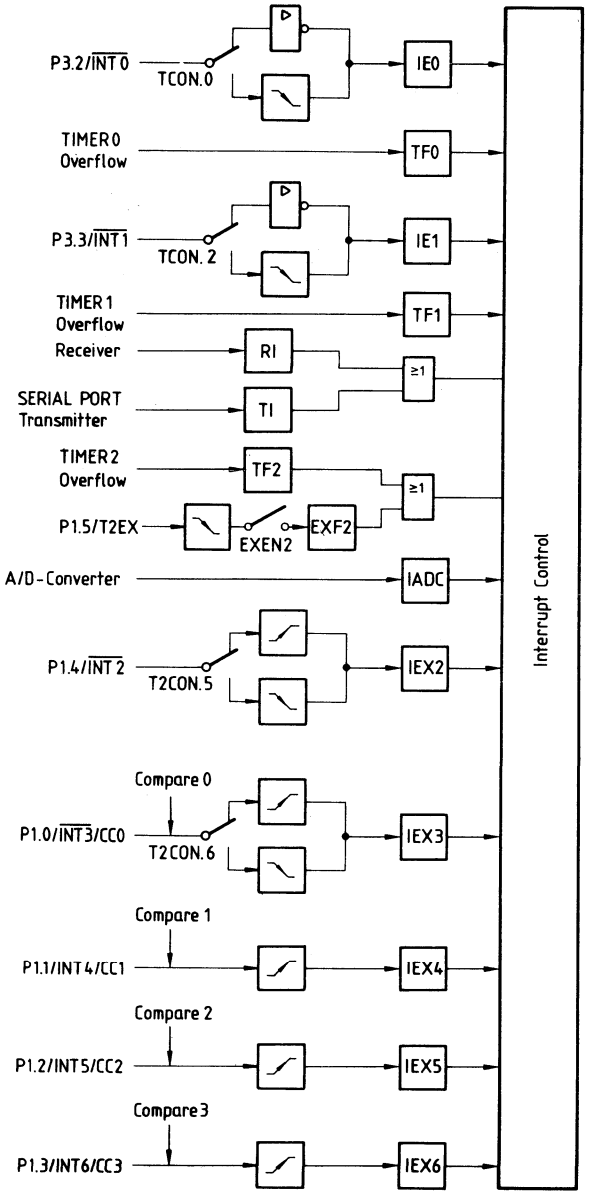
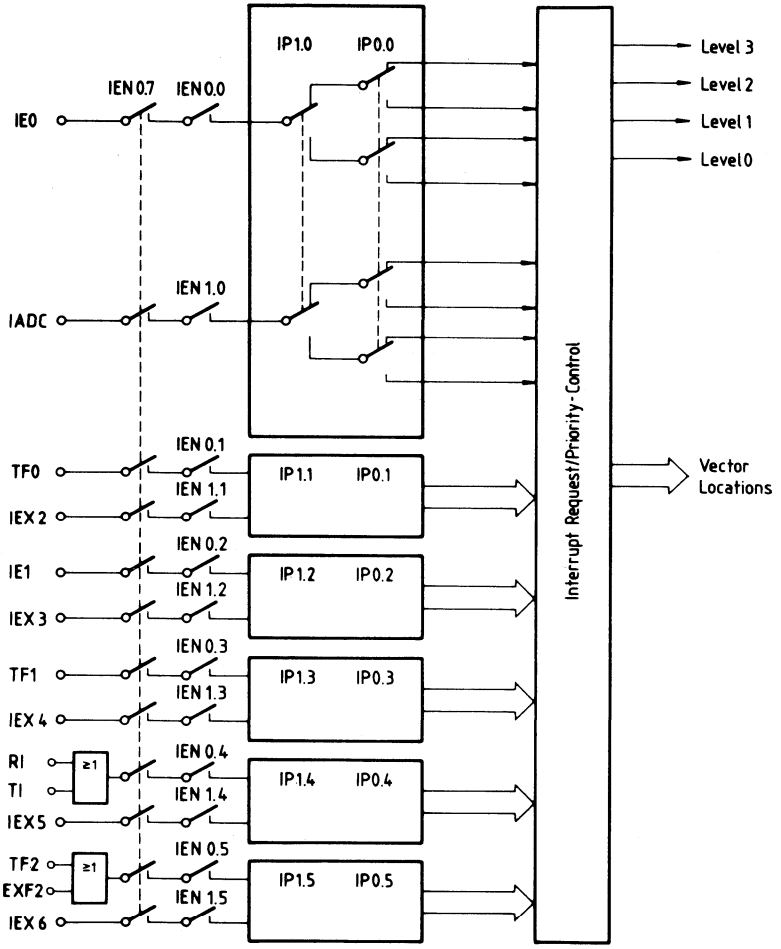


Figure 6
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN 0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	−0 to + 70°C for SAB 80515/80535
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $T_A = -0$ to $+70°C$; for SAB 80515/80535

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{RESET}$ and XTAL2)	2.0	$V_{CC}+0.5$	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	$V_{CC}+0.5$	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{RESET}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	$I_{OL} = 1.6\,mA$
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$	–	0.45	V	$I_{OL} = 3.2\,mA$
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	$I_{OH} = -80\,\mu A$
V_{OH1}	Output high voltage, port 0, ALE, $\overline{PSEN}$	2.4	–	V	$I_{OH} = -400\,\mu A$
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	−800	µA	$V_{IL} = 0.45\,V$
I_{IL2}	Logic 0 input current, XTAL2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45\,V$
I_{IL3}	Input low current to $\overline{RESET}$ for reset	–	−500	µA	$V_{IL} = 0.45\,V$
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	$0\,V < V_{IN} < V_{CC}$
I_{CC}	Power supply current SAB 80515/80535	–	210	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	$V_{CC} = 0\,V$
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1\,MHz$

A/D Converter Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V; V_{AREF} = V_{CC} ±5%; V_{AGND} = V_{SS} ±0.2V; $V_{IntAREF} - V_{IntAGND} \geq 1$V;
T_A = 0 to +70°C for SAB 80515/80535

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND}– 0.2	–	V_{AREF}+ 0.2	V	–
C_I	Analog input capacitance	–	25	–	pF	1)
t_L	Load time	–	–	2 t_{CY}	µs	–
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	µs	–
t_C	Conversion time (including sample time)	–	–	15 t_{CY}	µs	–
DNLE	Differential non-linearity	–	±1/2	±1	LSB	$V_{IntAREF}$ =
INLE	Integral non-linearity	–	±1/2	±1	LSB	V_{AREF} = V_{CC}
	Offset error		±1/2	±1	LSB	$V_{IntAGND}$ =
	Gain error		±1/2	±1	LSB	V_{AGND} = V_{SS}
TUE	Total unadjusted error		±1	±2	LSB	1)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)
$V_{IntREFERR}$	Internal reference error	–	±5	±15	mV	2)

Note 1): The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

Note 2): The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$
$T_A = 0°$ to $+70°C$ for SAB 80515/80535
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	12 t_{CLCL}	–	ns
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL}-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	4 t_{CLCL}-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	3 t_{CLCL}-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	3 t_{CLCL}-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	5 t_{CLCL}-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

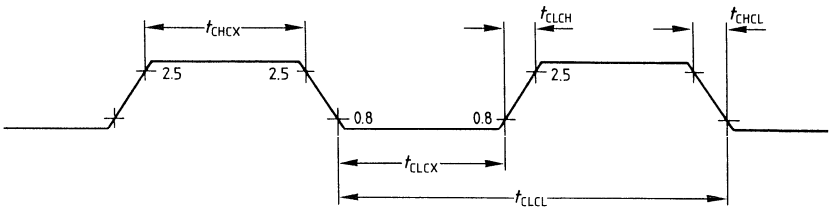
Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	6 t_{CLCL}-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	6 t_{CLCL}-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL}-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	5 t_{CLCL}-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	2 t_{CLCL}-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	8 t_{CLCL}-150	ns
t_{AVDV}	Address to valid data in	–	585	–	9 t_{CLCL}-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3 t_{CLCL}-50	3 t_{CLCL}+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4 t_{CLCL}-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	7 t_{CLCL}-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 80515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

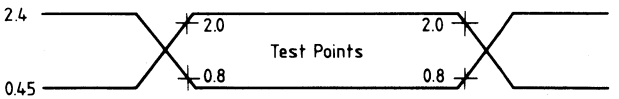
External Clock Drive XTAL2

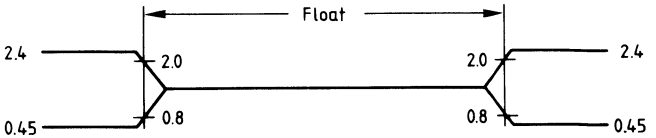
Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



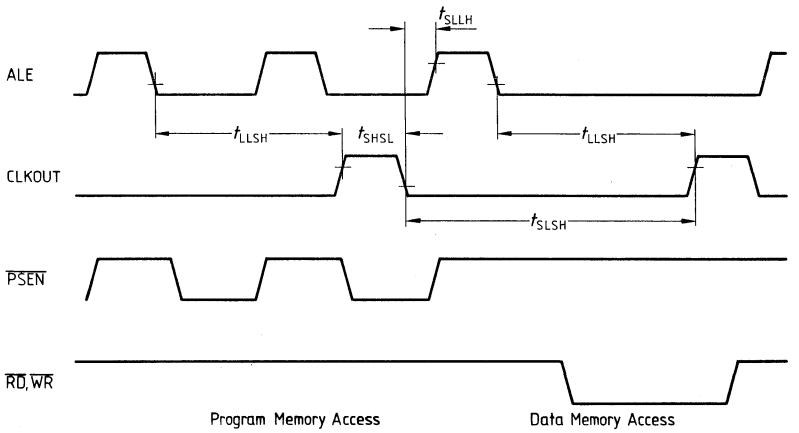


AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

System Clock Timing

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LLSH}	ALE to CLKOUT	543	–	7 t_{CLCL}-40	–	ns
t_{SHSL}	CLKOUT high time	127	–	2 t_{CLCL}-40	–	ns
t_{SLSH}	CLKOUT low time	793	–	10 t_{CLCL}-40	–	ns
t_{SLLH}	CLKOUT low to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns

System Clock Timing

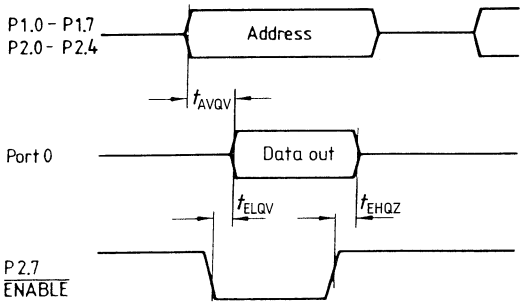


ROM Verification Characteristics

$T_A = 25°C \pm °C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0\ V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



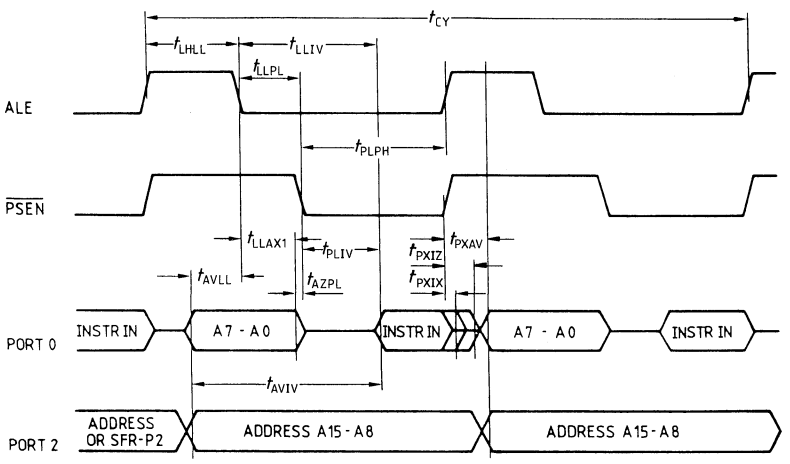
Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

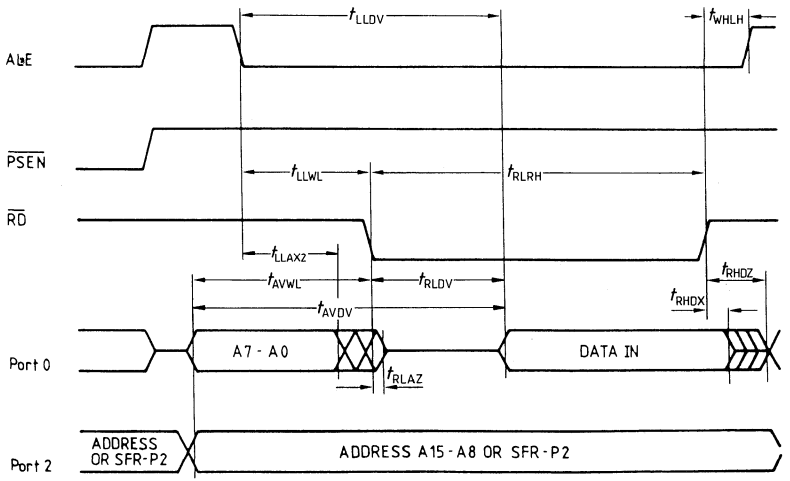
Inputs: P2.5–P2.6, $\overline{PSEN} = V_{SS}$
ALE, $\overline{EA} = V_{IH}$
$\overline{RESET} = V_{IL}$

Waveforms

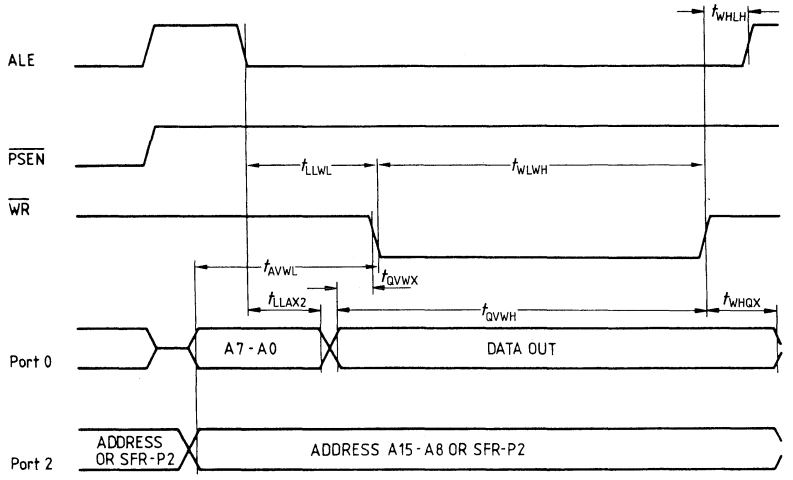
Program Memory Read Cycle



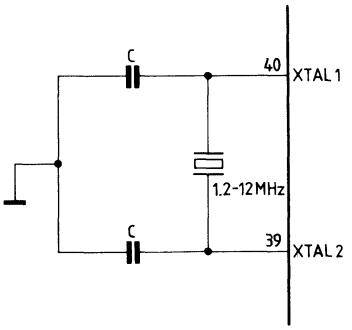
Data Memory Read Cycle



Data Memory Write Cycle

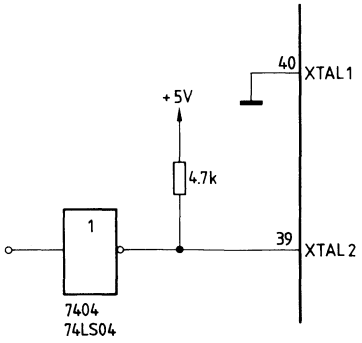


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

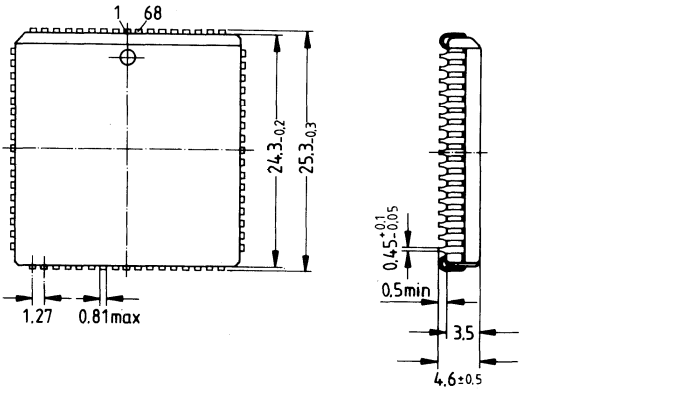
Crystal Oscillator Mode



Driving from External Source

Package Outlines

68-Pin Plastic Leaded Chip Carrier Package, PLCC 68



Dimensions in mm

Ordering Information

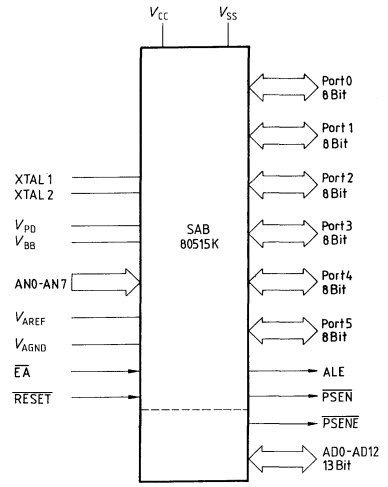
Type	Ordering code	Description
		8-bit single-chip microcontroller
SAB 80515-N	Q 67120-C211	with mask-programmable ROM (plastic)
SAB 80535-N	Q 67120-C241	for external memory (plastic)

Preliminary

SAB 80515K
8-Bit Single-Chip Microcontroller
ROM-less Version

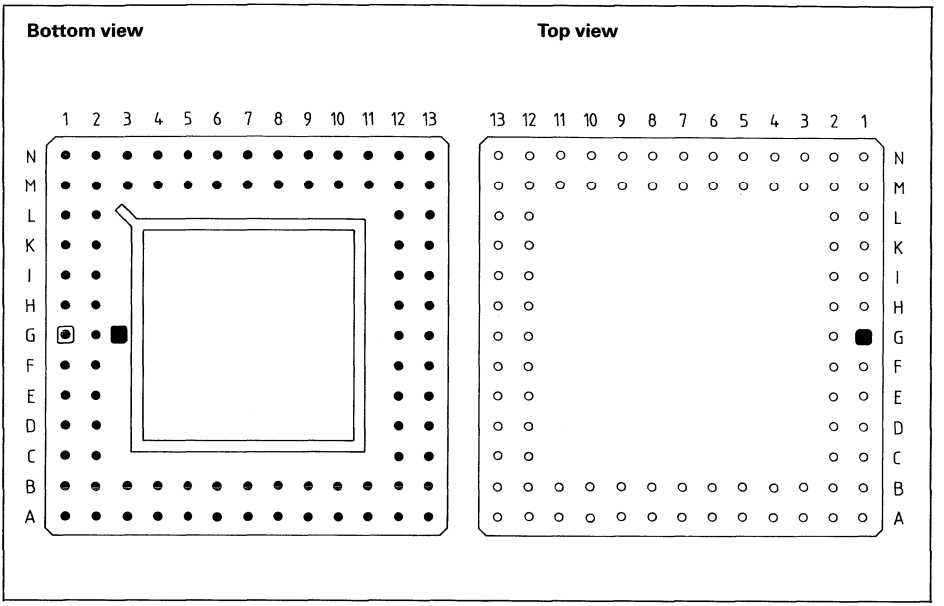
- Additional bus interface for external memory
- 256 × 8 RAM
- Six 8-bit ports
- Three 16-bit timer/event counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt sources, four priority levels
- 8-bit A/D converter with 8 multiplexed analog inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable to 128 Kbyte
- Pin grid array package, 88 pins (C-PGA-88)

Logic Symbol



The SAB 80515K is a special ROM-less version of the 8-bit microcontroller SAB 80515. The SAB 80515K contains an additional bus interface to connect an external program memory in place of the SAB 80515's on-chip ROM. Thereby, the SAB 80515K maintains the full I/O capability of the single-chip SAB 80515 while it permits connection of an external program memory. All other features of the SAB 80515K are identical with those of the SAB 80515.
The SAB 80515K is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology, and supplied as pin grid array with 88 pins (C-PGA-88).

Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12	J 13 J 12 K 13 K 12 L 13 M 13 L 12 N 13 N 8 M 7 N 7 M 6 N 6	I/O	Multiplexed address/data bus for the program memory. This bus is used for connecting an external memory in place of the 8-Kbyte internal ROM of the SAB 80515. Pins AD0 to AD12 can sink/source 5 LS-TTL loads.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	A 8 B 8 A 7 B 7 A 6 B 6 A 5 B 5	I	Multiplexed analog inputs of the A/D converter.
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	N 1 M 2 L 2 M 1 K 2 L 1 K 1 J 2	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external program and data memory. Port 0 can sink/source 8 LS-TTL loads.
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	F 13 F 12 E 13 E 12 D 13 C 13 D 12 B 13	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input – $\overline{\text{INT2}}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input.

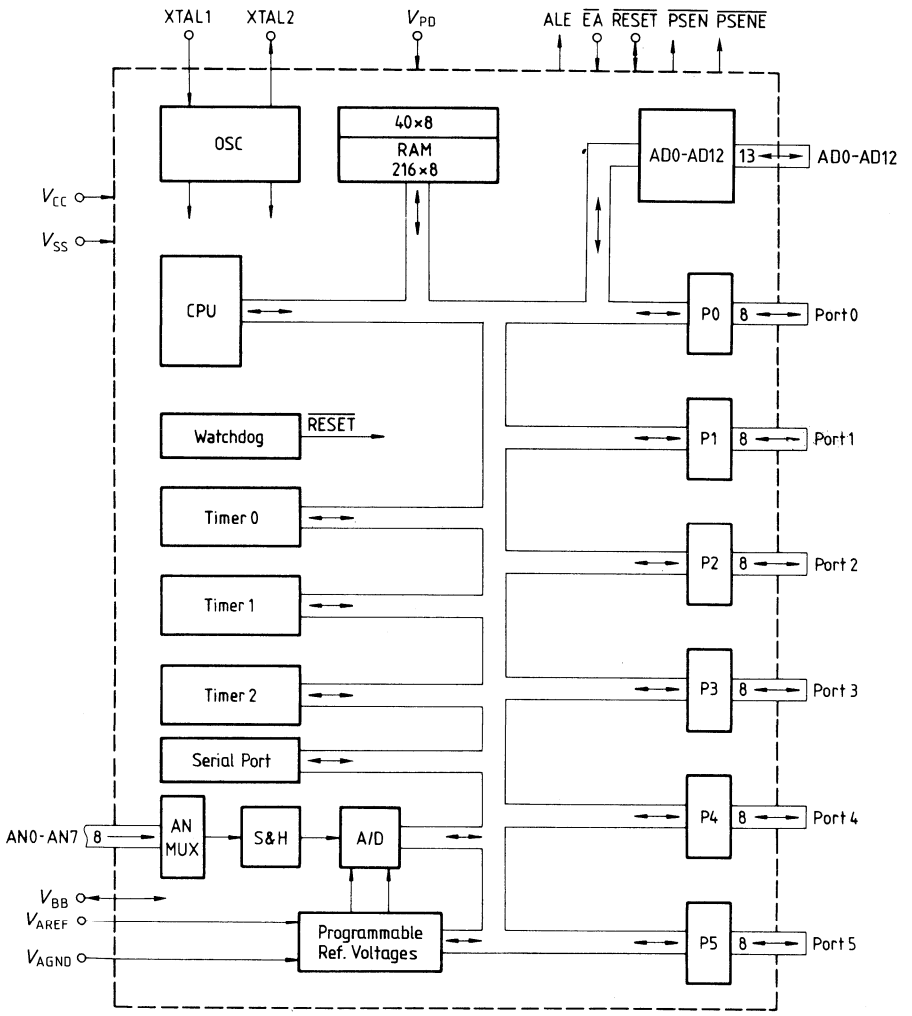
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	M 11 N 12 M 10 N 11 N 10 M 9 N 9 M 8	I/O	Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application, port 2 employs strong internal pullup resistors when issuing 1 s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register. Port 2 can sink/source 4 LS-TTL loads.
P3.0 P3.1 P3.2 P3.3 P3.4 P3.5 P3.6 P3.7	A 9 B 9 A 10 B 10 A 11 A 12 B 12 C 12	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$ (P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0.
P4.0 P4.1 P4.2 P4.3 P4.4 P4.5 P4.6 P4.7	D 1 D 2 C 1 C 2 A 1 B 2 B 3 A 2	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
P5.0 P5.1 P5.2 P5.3 P5.4 P5.5 P5.6 P5.7	E 1 F 1 F 2 G 1 G 2 H 1 H 2 J 1	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
XTAL2 XTAL1	H 12 H 13		XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flipflop. Minimum and maximum high and low times specified in the AC characteristics must be observed. XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{RESET}}$	B 4	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515K. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
ALE	N 2	O	Provides ADDRESS LATCH ENABLE output used for latching the address into external memories at port 0 and 2, and AD0-AD12. It is activated every six oscillator periods except during external data memory accesses.
$\overline{\text{PSEN}}$	N 3	O	The PROGRAM STORE ENABLE output is a control signal that enables the external program memory at port 0 and 2 to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during program execution from program memory at AD0-AD12.
$\overline{\text{PSENE}}$	M 12	O	This output is a control signal that enables the program memory at AD0-AD12 during instruction fetch operations. It is activated every six oscillator periods.
$\overline{\text{EA}}$	M 3	I	When $\overline{\text{EA}}$ is held at a TTL high level, the SAB 80515K executes instructions from the program memory that is connected to AD0-AD12 when the PC is less than 8192. When $\overline{\text{EA}}$ is held at a TTL low level, the SAB 80515K executes all instructions from external program memory.
V_{AREF}	A 3		Reference voltage for the A/D converter
V_{AGND}	A 4		Reference ground for the A/D converter
V_{CC}	E 2		POWER SUPPLY (+5V power supply during normal operation and program verification)
V_{SS}	G 13		GROUND (0V)
V_{PD}	B 1		POWER DOWN SUPPLY. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 bytes of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
V_{BB}	G 12		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 1000 nF) for proper operation of the A/D converter.
NC	A 13 B 11 M 4 M 5 N 4 N 5		No connection.

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515 with factory mask-programmable 8 Kbyte on-chip ROM
- SAB 80535 ROM-less version of the SAB 80515
- SAB 80515K ROM-less version of the SAB 80515 with additional bus interface.

In this data sheet the term "SAB 80515" is used to refer generally to all members of the SAB 80515 family, except where specifically stated otherwise.

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- instruction set
- external memory expansion interface (port 0 and port 2)
- full-duplex serial port
- timer/counters 0 and 1
- alternate functions on port 3
- the lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

Different to the SAB 8051 are the RAM power-down supply, which supplies 40 byte with a typical current of 2 mA, and the powerful interrupt structure with 12 sources and 4 priority levels.
The SAB 80515 additionally contains 128 byte of internal RAM and 4 Kbyte of internal ROM, that means a total of 256 byte RAM and 8 Kbyte ROM (SAB 80515 only) on-chip. The SAB 80515 has a 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with 8 analog inputs and programmable reference voltages, two additional quasi-bidirectional 8-bit ports, and a programmable clock output ($f_{osc}/12$).
The SAB 80515K is a special ROM-less version of the SAB 80515. In place of the 8 Kbyte on-chip ROM there is an additional bus interface for an 8 Kbyte program memory which can be connected externally.

Figure 2 shows a detailed block diagram of the SAB 80515K.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities of binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described below.

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbyte. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this device.

The SAB 80515K has the same function as the SAB 80515; the difference is that fetches from the internal ROM are executed from a program memory via the additional bus interface (AD0-AD12).

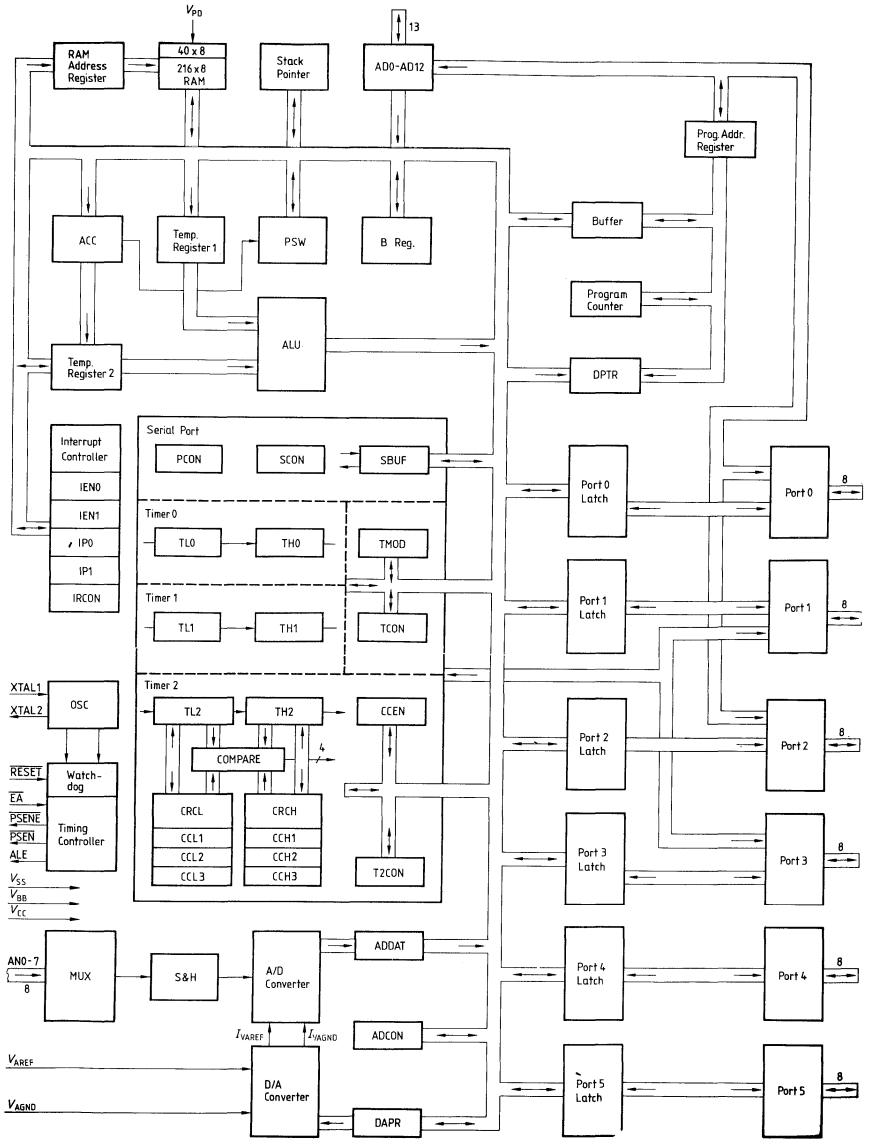
Data memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 byte of RAM; the upper 128 byte of RAM; and the 128-byte special function register (SFR) area. While the upper 128 byte of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 byte of data memory can be accessed through direct or register-indirect addressing; the upper 128 byte of RAM can be accessed through register-indirect addressing; and the special function registers are accessed through direct addressing.

Four 8-register banks occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depths can be expanded up to 256 byte.

The external data memory can be expanded up to 64 Kbyte and can be accessed by instructions that use a 16-bit or an 8-bit address.

Figure 2
Detailed Block Diagram



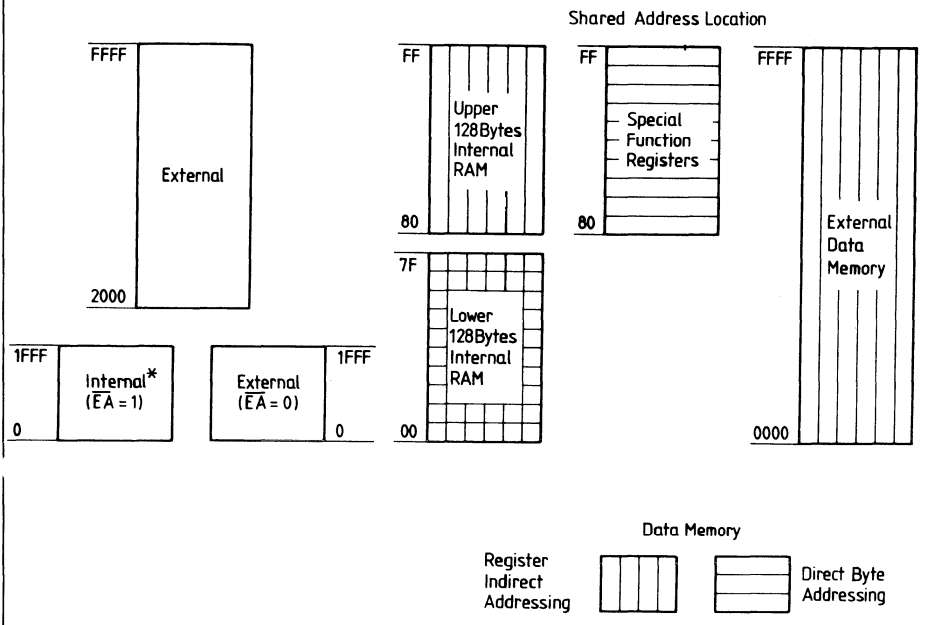
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D converter control register	0D8H
ADDAT	A/D converter data register	0D9H
DAPR	D/A converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.

Figure 3 illustrates the memory address spaces of the SAB 80515.

Figure 3
Memory Address Spaces



*) Additional program memory of the SAB 80515K at AD0-AD12

I/O Ports

The SAB 80515 has six 8-bit ports. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-ups. That means, when configured as inputs, ports 1 to 5 will pull high, and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial input port
P3.1	TXD	Serial output port
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

–Timer/counters 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler
Mode 1: 16-bit timer/counter
Mode 2: 8-bit timer/counter with 8-bit auto-reload
Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

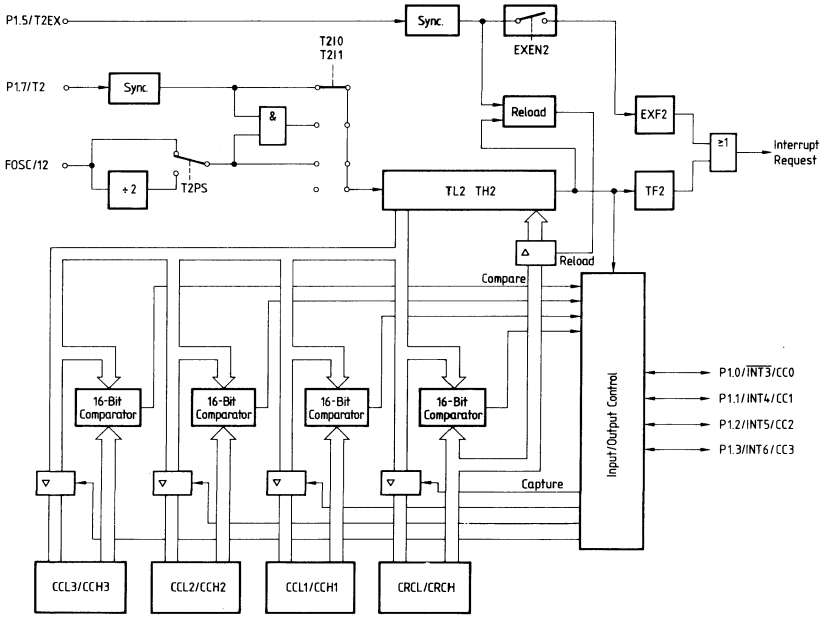
External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

–Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin on port 1 for capture input/compare output.

Figure 4 shows a block diagram of timer/counter 2.

Figure 4
Block Diagram of Timer/Counter 2



Reload

With the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH, a 16-bit reload can be performed. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).
Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.
Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Serial Port

The serial port of the SAB 80515 permits the full duplex communication between microcontrollers or between microcontrollers and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.
Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.
Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.
Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

The variable baud rates can be generated by timer 1 or an internal baud rate generator.

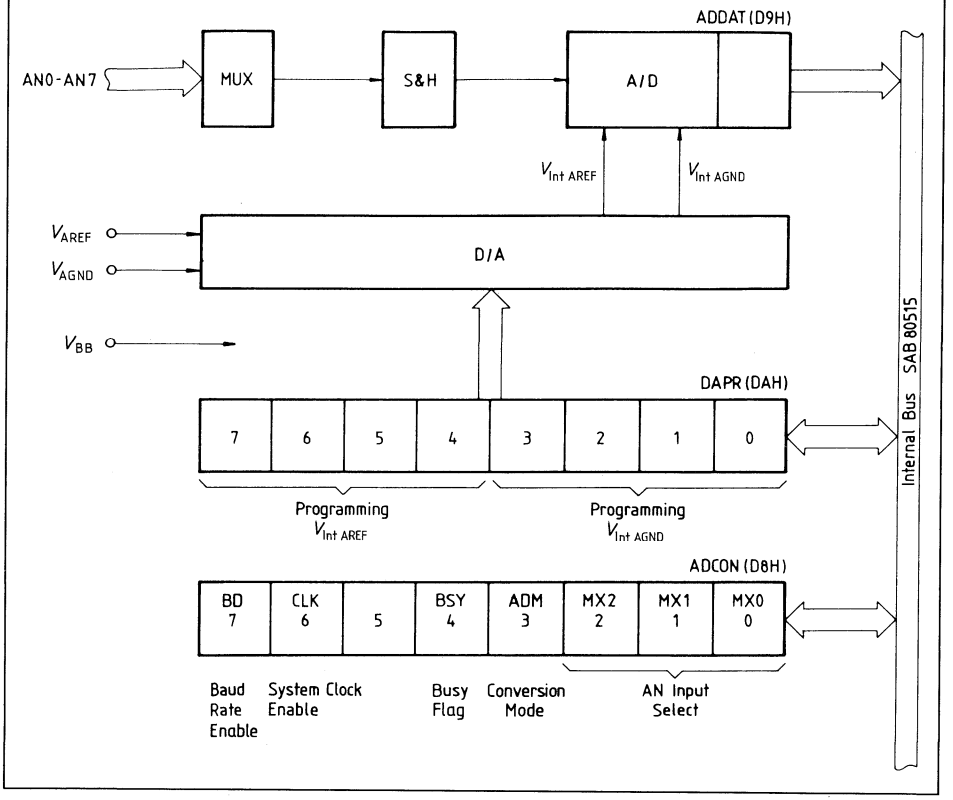
A/D Converter

The 8-bit A/D converter of the SAB 80515 has 8 multiplexed analog inputs and is using the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated.

The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter are programmable in 16 steps with respect to the external reference voltages. This feature permits a second conversion with changed internal reference voltages to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog voltage range. Takes 7 machine cycles each (7 µs at 12 MHz oscillator frequency).

Figure 5 shows a block diagram of the A/D converter of the SAB 80515.

Figure 5
A/D Converter Block Diagram



Interrupt Structure

The 12 interrupt sources of the SAB 80515 are organized in 6 pairs:

External interrupt 0	–	A/D converter interrupt
Timer 0 interrupt	–	External interrupt 2
External interrupt 1	–	External interrupt 3
Timer 1 interrupt	–	External interrupt 4
Serial port interrupt	–	External interrupt 5
Timer 2 interrupt	–	External interrupt 6

Each interrupt source has its own vector address. It can be programmed to one of four priority levels and can individually be enabled/disabled. The minimum interrupt response time is 3 to 8 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed to be activated by a negative or a positive transition. The external interrupts 4 to 6 are activated by a positive transition. The interrupts 3 to 6 can be combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

Figure 6 shows the interrupt request sources, and figure 7 illustrates the priority level structure of the SAB 80515.

Figure 6
Interrupt Request Sources

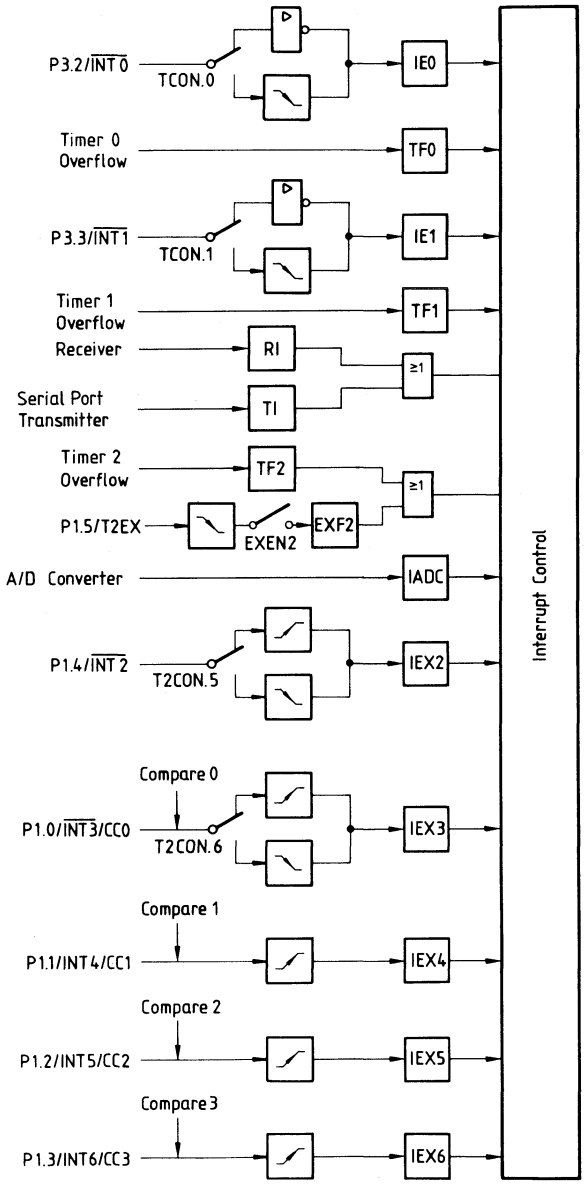
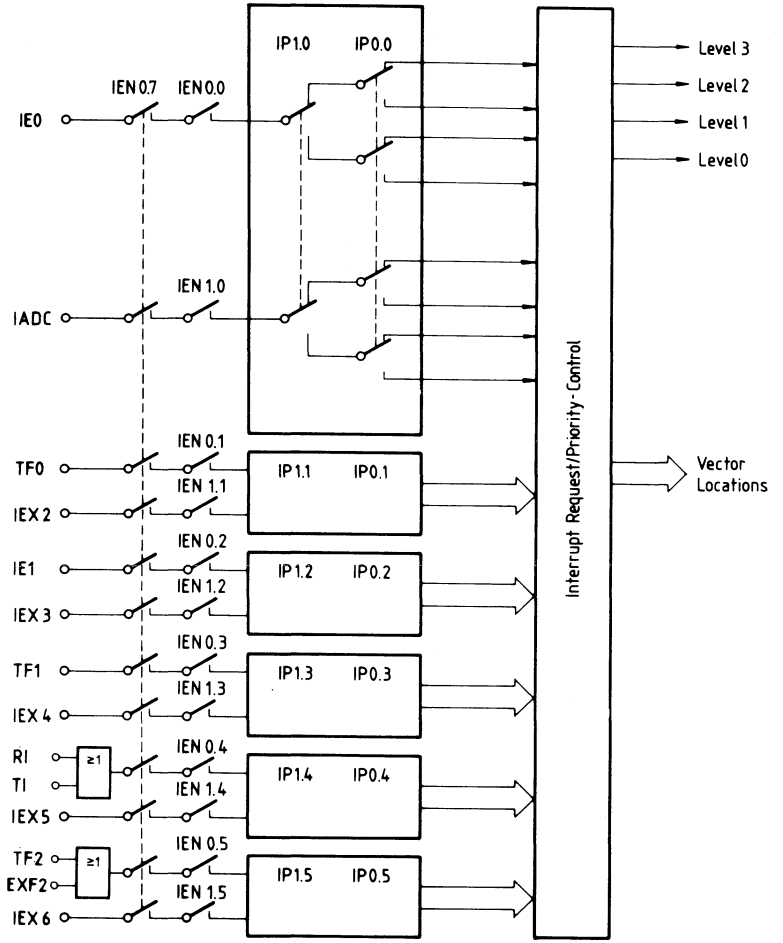


Figure 7
Priority Level Structure



Watchdog Timer

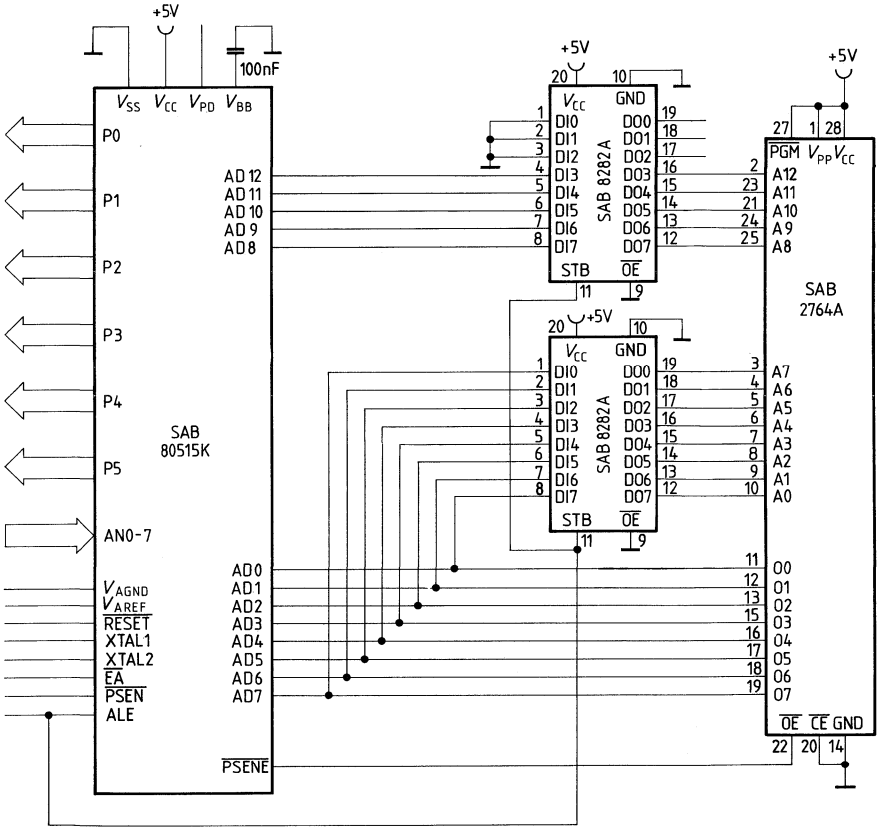
This feature is provided as a means of graceful recovery from software upset. After a reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65536 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), a hardware reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions. This is done to prevent the watchdog from being cleared by unexpected op codes.

Connecting an External Program Memory to the SAB 80515K

The ROM-less chip SAB 80515K allows emulating the SAB 80515's internal ROM via the additional bus interface. The multiplexed bus AD0 to AD12 emits the address and reads the instruction at pins AD0 to AD7. Observe that the higher address lines AD8 to AD12 are also multiplexed. The control signals for the emulation memory are ALE and $\overline{\text{PSENE}}$.

When pin $\overline{\text{EA}}$ is high, the SAB 80515K executes instructions read from AD0-AD12 if the PC is less than 8192, otherwise it will execute from external program memory at port 0 and 2. When pin $\overline{\text{EA}}$ is low, the SAB 80515K executes all instructions from external program memory. Figure 8 shows a typical circuitry for connection of a program memory to AD0-AD12 of the SAB 80515K.

Figure 8
Connecting an External Program Memory



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	2
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate accumulator right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Data transfer

MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn — Working register R0–R7
direct — 128 internal RAM locations, any I/O port, control or status register
@Ri — Indirect internal or external RAM location addressed by register R0 or R1
#data — 8-bit constant included in instruction
#data 16 — 16-bit constant included as bytes 2 and 3 of instruction
bit — 128 software flags, any I/O pin, control or status bit
A — Accumulator

Notes on program addressing modes:

addr 16 — Destination address for LCALL and LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11 — Destination address for ACALL and AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex code	Number of bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $T_A = 0$ to 70°C

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{RESET}$ and XTAL2)	2.0	V_{CC}+0.5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC}+0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{RESET}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	$I_{OL} = 1.6$ mA
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PSENE}$	–	0.45	V	$I_{OL} = 3.2$ mA
V_{OL2}	Output low voltage, AD0 to AD12	–	0.45	V	$I_{OL} = 2$ mA
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	$I_{OH} = -80\,\mu A$
V_{OH1}	Output high voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PSENE}$	2.4	–	V	$I_{OH} = -400\,\mu A$
V_{OH2}	Output high voltage, AD0 to AD12	2.4	–	V	$I_{OH} = -2$ mA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	−800	µA	$V_{IL} = 0.45\,V$
I_{IL2}	Logic 0 input current, XTAL2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45\,V$
I_{IL3}	Input low current to $\overline{RESET}$ for reset	–	−500	µA	$V_{IL} = 0.45\,V$
I_{LI}	Input leakage current to port 0, $\overline{EA}$, AD0 to AD12	–	±10	µA	$0\,V < V_{IN} < V_{CC}$
I_{CC}	Power supply current	–	210	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	$V_{CC} = 0\,V$
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1$ MHz

A/D Converter Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $V_{AREF} = V_{CC} \pm 5\%$; $V_{AGND} = V_{SS} \pm 0.2\,V$; $V_{IntAREF} - V_{IntAGND} \geq 1\,V$;
$T_A = 0$ to $+70°C$ for SAB 80515K

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	$V_{AGND}-$ 0.2	–	$V_{AREF}+$ 0.2	V	–
C_I	Analog input capacitance	–	25	–	pF	1)
t_L	Load time	–	–	$2t_{CY}$	µs	–
t_S	Sample time (incl. load time)	–	–	$5t_{CY}$	µs	–
t_C	Conversion time (incl. sample time)	–	–	$15t_{CY}$	µs	–
DNLE	Differential non-linearity	–	±1/2	±1	LSB	$V_{IntAREF} =$
INLE	Integral non-linearity	–	±1/2	±1	LSB	$V_{AREF} = V_{CC}$
	Offset error	–	±1/2	±1	LSB	$V_{IntAGND} =$
	Gain error	–	±1/2	±1	LSB	$V_{AGND} = V_{SS}$
TUE	Total unadjusted error	–	±1	±2	LSB	1)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)
$V_{IntREFERR}$	Internal reference error	–	–	TBD	mV	2)

1) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V
(C_L for port 0, ALE, $\overline{PSEN}$ and $\overline{PSENE}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics at Port 0/Port 2

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL1}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV1}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL1}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH1}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV1}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX1}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ1} [4]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV1} [4]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV1}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL1}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{DVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

[4] Interfacing the SAB 80515K to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

Program Memory Characteristics at AD0-AD12

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL2}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX3}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV2}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL2}	ALE to $\overline{\text{PSENE}}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH2}	$\overline{\text{PSENE}}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV2}	$\overline{\text{PSENE}}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX2}	Input instruction hold after $\overline{\text{PSENE}}$	0	–	0	–	ns
t_{PXIZ2} [5]	Input instruction float after $\overline{\text{PSENE}}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV2} [5]	Address valid after $\overline{\text{PSENE}}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV2}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL2}	Address float to $\overline{\text{PSENE}}$	0	–	0	–	ns

External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

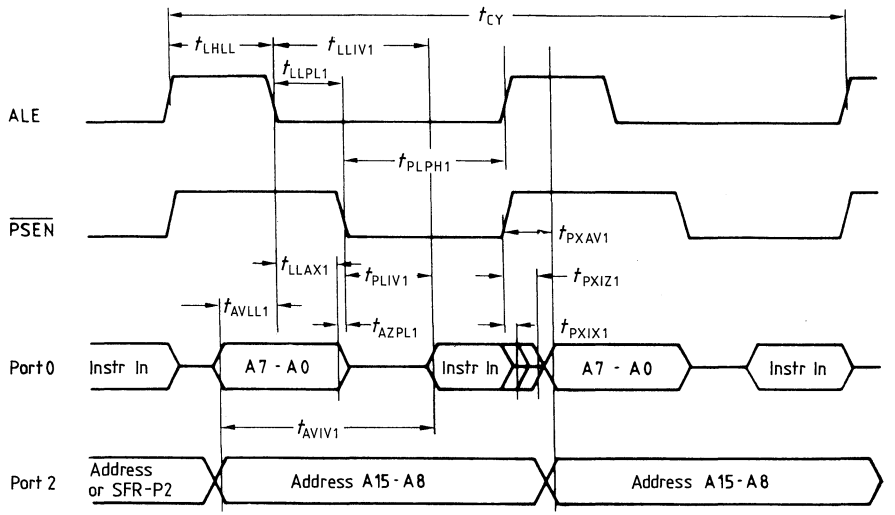
System Clock Timing

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LLSH}	ALE to CLKOUT	543	–	$7t_{CLCL}$-40	–	ns
t_{SHSL}	CLKOUT high time	127	–	$2t_{CLCL}$-40	–	ns
t_{SLSH}	CLKOUT low time	793	–	$10t_{CLCL}$-40	–	ns
t_{SLLH}	CLKOUT low to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns

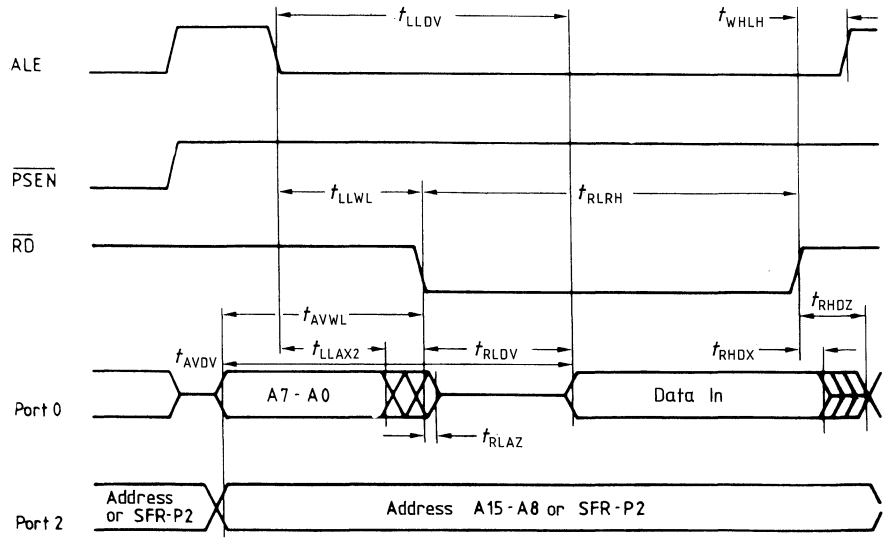
[5] Interfacing the SAB 80515K to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to AD0–AD7 drivers.

Waveforms

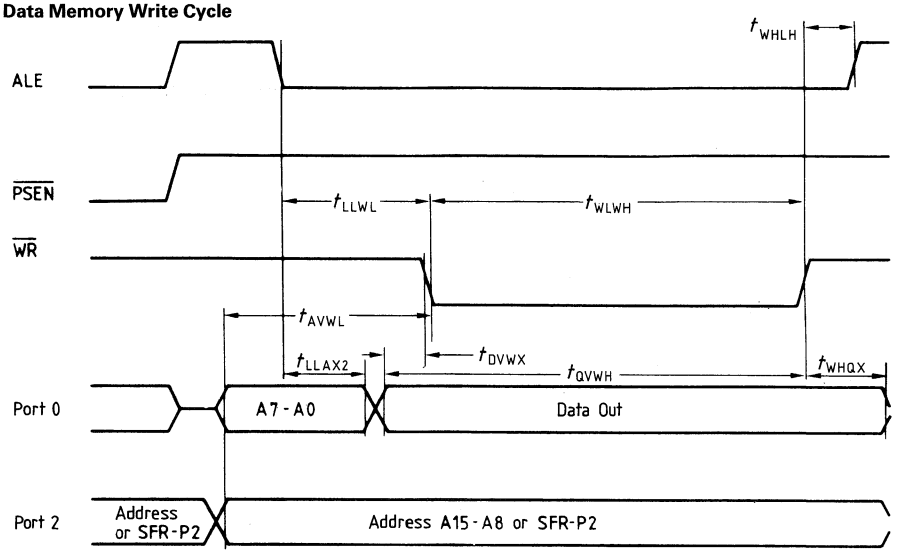
Program Memory Read Cycle at Port 0 / Port 2



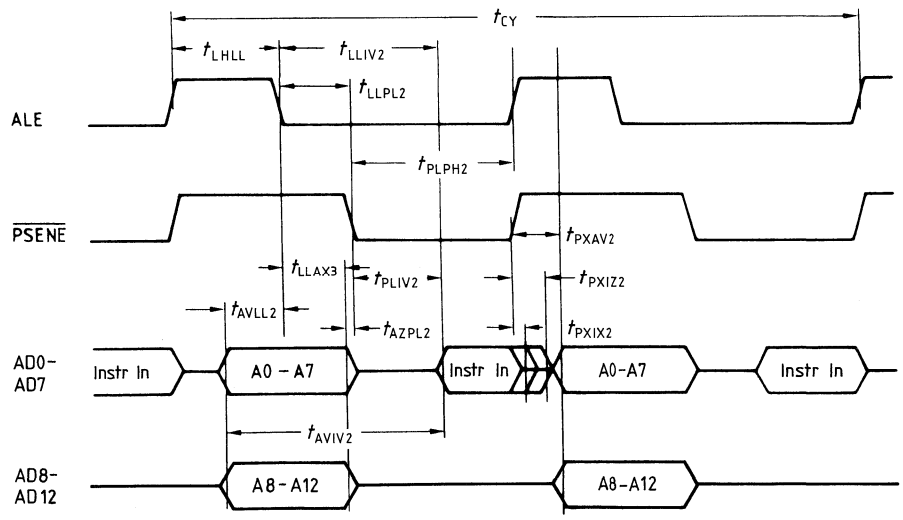
Data Memory Read Cycle



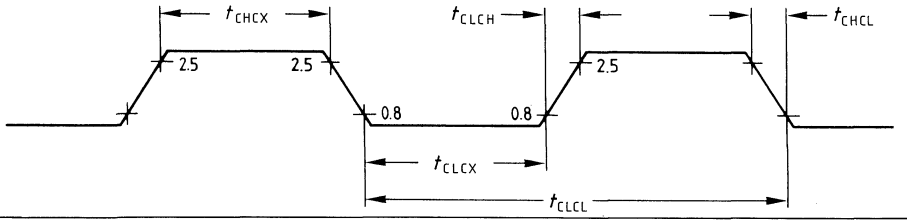
Data Memory Write Cycle



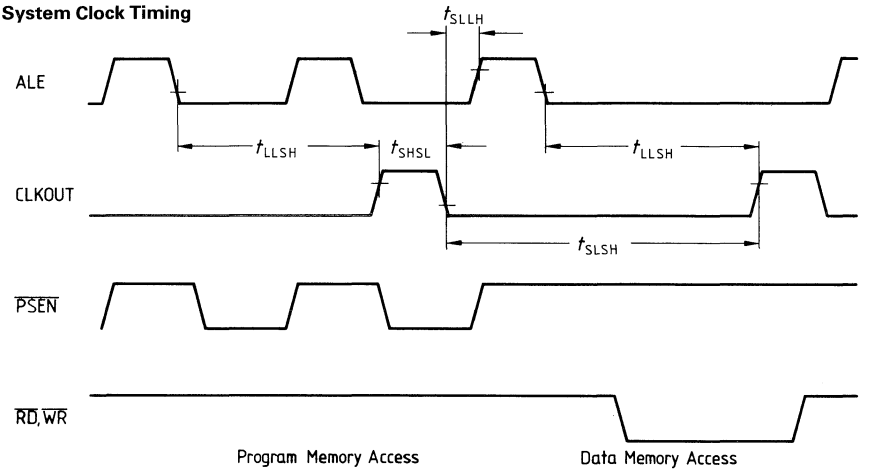
Emulation Memory Read Cycle at AD0-AD12



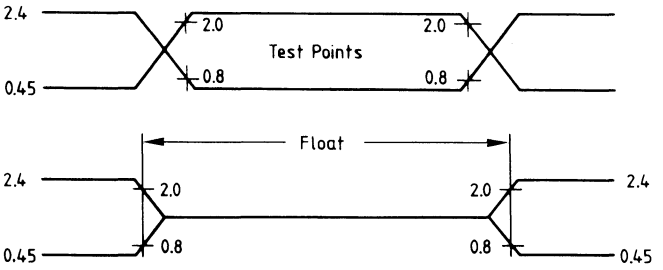
External Clock Cycle



System Clock Timing

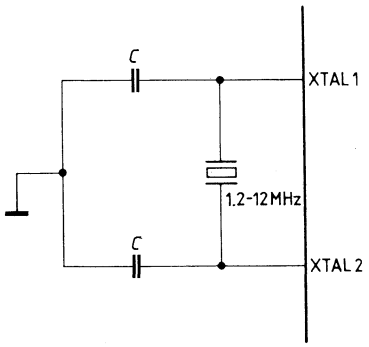


AC Testing Input, Output, Float Waveforms



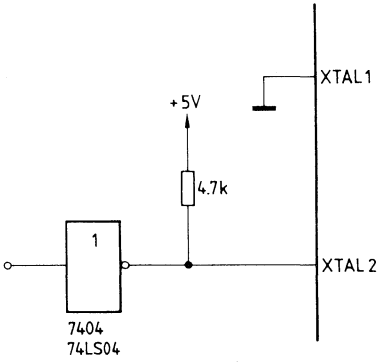
AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pins sinks 3.2 mA or sources 400 µA at voltage test levels.

Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

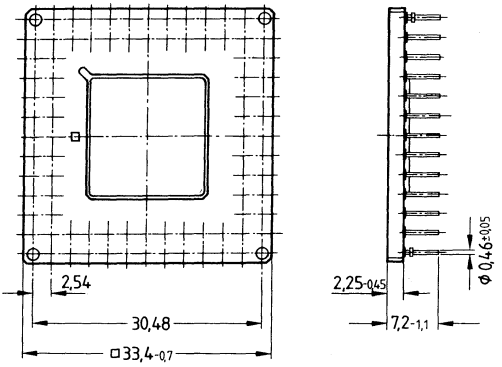
Crystal Oscillator Mode



Driving from External Source

Package Outlines

Pin Grid Array, C-PGA-88



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 80515K-A	Q67120-C267	8-bit single-chip microcontroller, ROM-less version

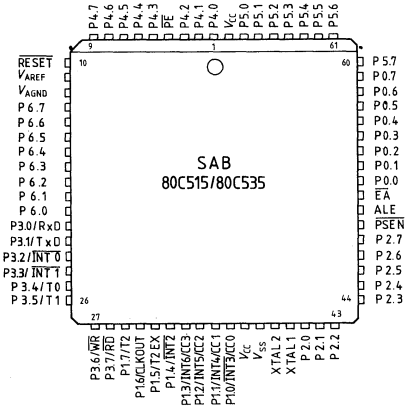
Advance Information

SAB 80C515/80C535
8-Bit CMOS Microcontroller

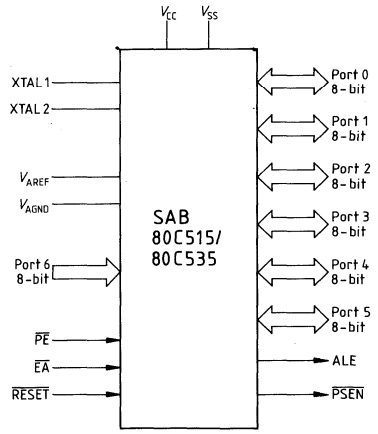
SAB 80C515 CMOS microcontroller with factory mask-programmable ROM
SAB 80C535 CMOS microcontroller for external ROM
SAB 80C515-T40/85
SAB 80C535-T40/85 Extended temperature range: −40 to +85°C

- 8K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one input port for digital or analog input
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Functionally compatible with SAB 80515 (NMOS)
- Idle and power-down mode
- 68-pin plastic leaded chip carrier package (PL-CC-68)

Pin Configuration
PL-CC-68



Logic Symbol



The SAB 80C515/80C535 is a new, powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is designed in Siemens ACMOS technology and is functionally compatible with the SAB 80515/80535 devices designed in MYMOS technology.
The SAB 80C515/80C535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051/80C51 architecture. While maintaining all the SAB 80C51 operating characteristics, the SAB 80C515/80C535 incorporates several enhancements which significantly increase design flexibility and overall system performance.

In addition, the low-power properties of Siemens ACMOS technology allow applications where power consumption and dissipation are critical. Furthermore, the SAB 80C515/80C535 has two software-selectable modes of reduced activity for further power reduction: idle and power-down mode.
The SAB 80C535 is identical with the SAB 80C515 except that it lacks the on-chip program memory.
The SAB 80C515/80C535 is supplied in a 68-pin plastic leaded chip carrier package (PL-CC-68).
For the industrial temperature range −40 to +85°C, the SAB 80C515/80C535-T40/85 is available.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.
$\overline{PE}$	4	I	A low level on this pin enables the use of the power saving modes (idle mode and power-down mode). When $\overline{PE}$ is held on high level it is impossible to enter the power saving modes.
$\overline{RESET}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
P6.7-P6.0	13-20	I	Port 6 is an 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels simultaneously meet the specifications for high/low input voltages and for the eight multiplexed analog inputs of the A/D converter.
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{INT1}$ (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

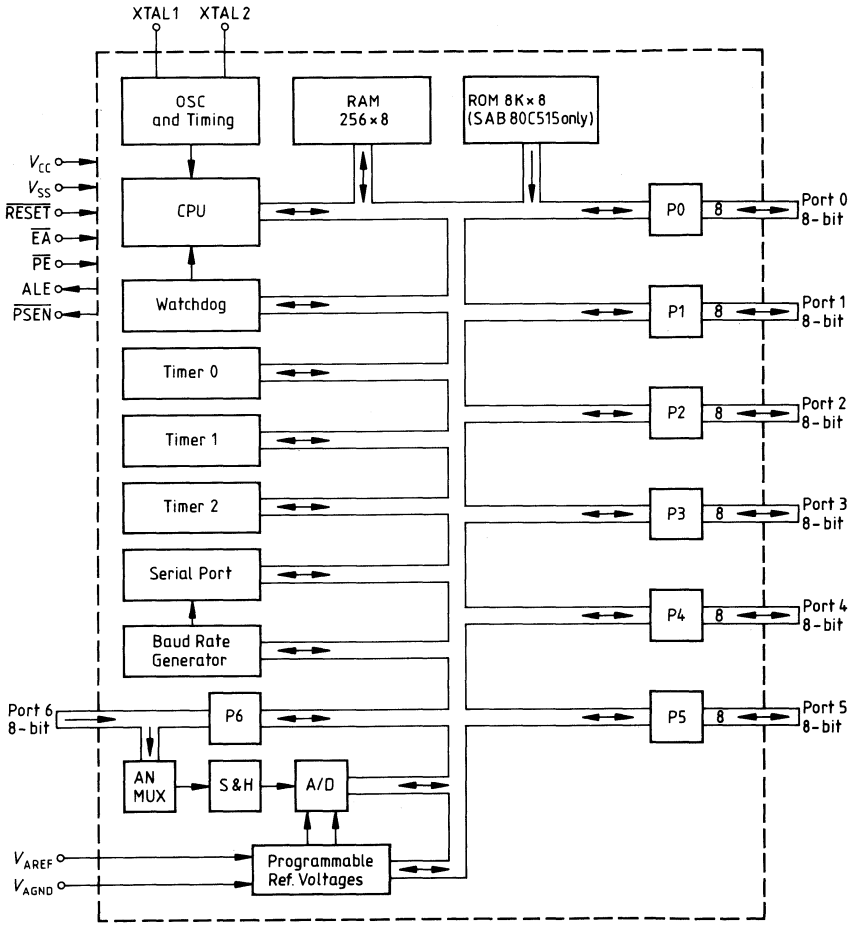
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{INT3}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input – $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{CC}	37		Supply voltage during normal, idle, and power down operation. Internally connected to pin 68.
V_{SS}	38		GROUND (0V)
XTAL2 XTAL1	39 40		XTAL2 Input to the inverting oscillator amplifier and input to the internal clock generator circuits. XTAL1 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.
$\overline{EA}$	51	I	When held high, the SAB 80C515 executes instructions from the internal ROM as long as the PC is less than 8192. When held low, the SAB 80C515 fetches all instructions from external program memory. For the SAB 80C535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C515. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.
V_{CC}	68		Supply voltage during normal, idle and power-down operations. Internally connected to pin 37.

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via this interface substitutes the SAB 80515's internal ROM.

The SAB 80C535 is identical to the SAB 80C515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80C515" is used to refer to both the SAB 80C515 and SAB 80C535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80C515 is based on the SAB 8051/SAB 80C51 microcontroller family. The following features of the SAB 80C515 are fully compatible with the SAB 80C51 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80C515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80C515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog or digital signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80C515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80C515.

CPU

The SAB 80C515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80C515 manipulates operands in the four memory address spaces described below:
(Figure 2 illustrates the memory address spaces of the SAB 80C515).

Program memory

The SAB 80C515 has 8 Kbyte of on-chip ROM, while the SAB 80C535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80C515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80C515 fetches all instructions from the external program memory. Since the SAB 80C535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

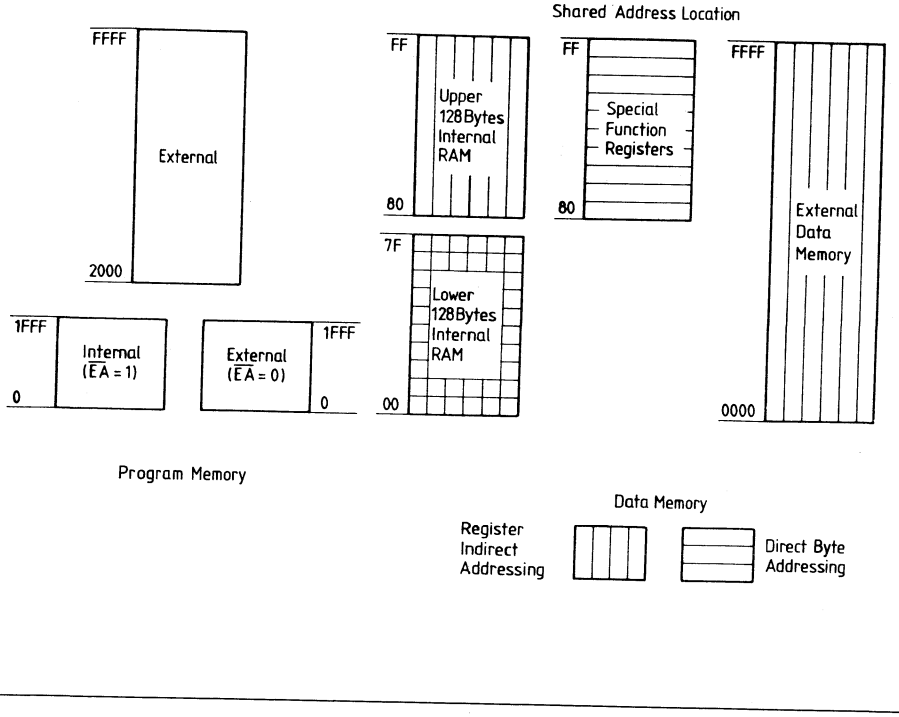
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 42 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1.

Table 1
Special Function Registers

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial channel control register	98H
SBUF	Serial channel buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D converter control register	0D8H
ADDAT	A/D converter data register	0D9H
DAPR	D/A converter program register	0DAH
P6	Port 6	0DBH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B-register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 80C515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{INT3}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{INT2}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	$\overline{TXD}$	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{INT0}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{INT1}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{WR}$	External data memory write strobe
P3.7	$\overline{RD}$	External data memory read strobe

The SAB 80C515 has a dual-purpose input port. As the ANx lines in the SAB 80515 (NMOS version), the eight port lines at port 6 can be used as analog inputs. But if the input voltages at port 6 meet the specified digital input levels (V_{IL} and V_{IH}), the port can also be used as digital input port. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6. It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their respective V_{IL}/V_{IH} specifications. Furthermore, it is not possible to use port P6 as output lines. Special function register P6 is located at address 0DBH.

Timer/Counters

The SAB 80C515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/counter 2

Timer/counter 2 of the SAB 80C515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 3 shows a block diagram of the timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

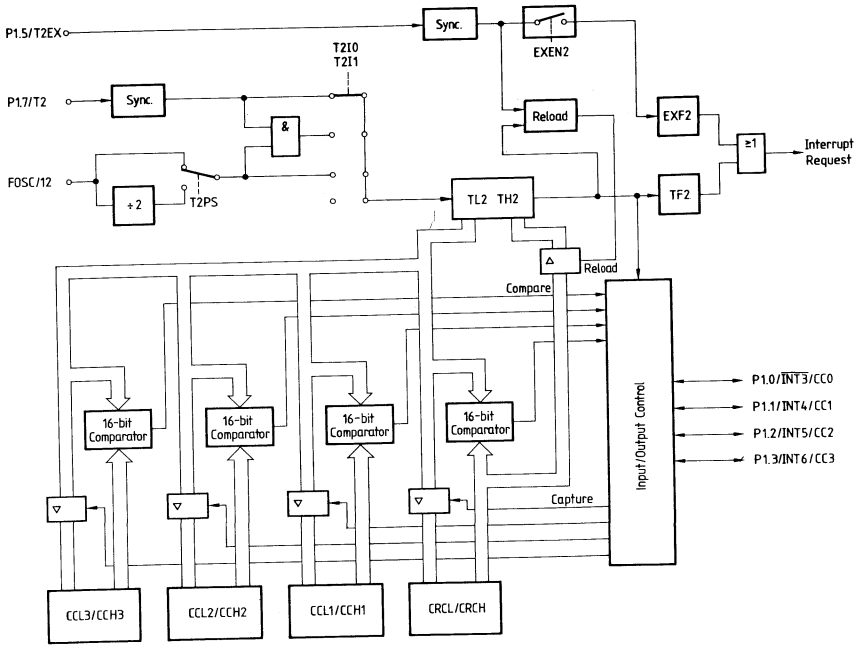
Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 80C515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

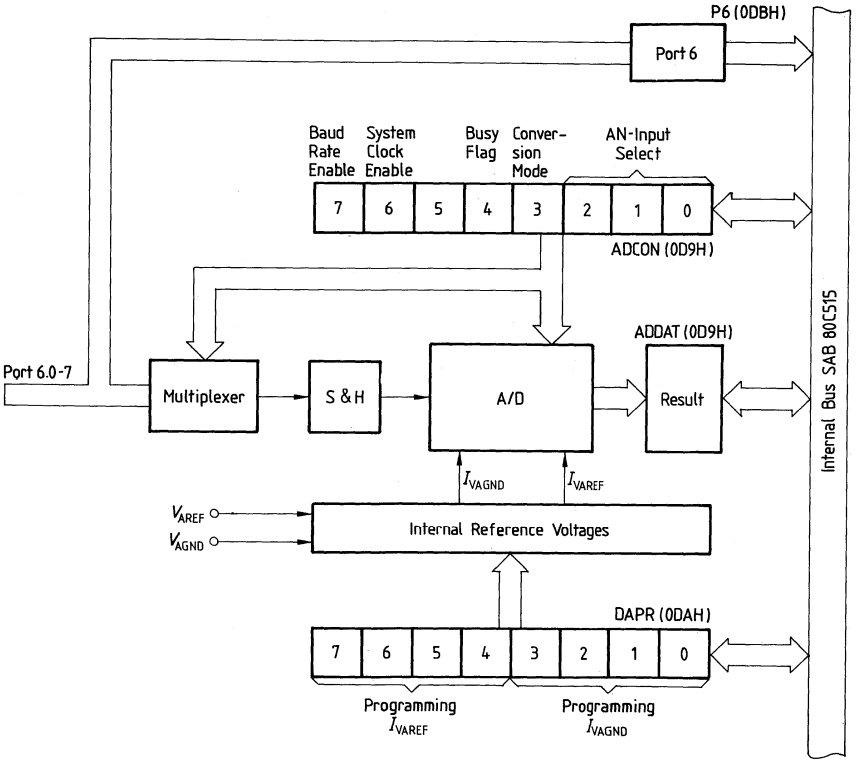
A/D Converter

The 8-bit A/D converter of the SAB 80C515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 14 machine cycles (14 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 80C515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/ disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

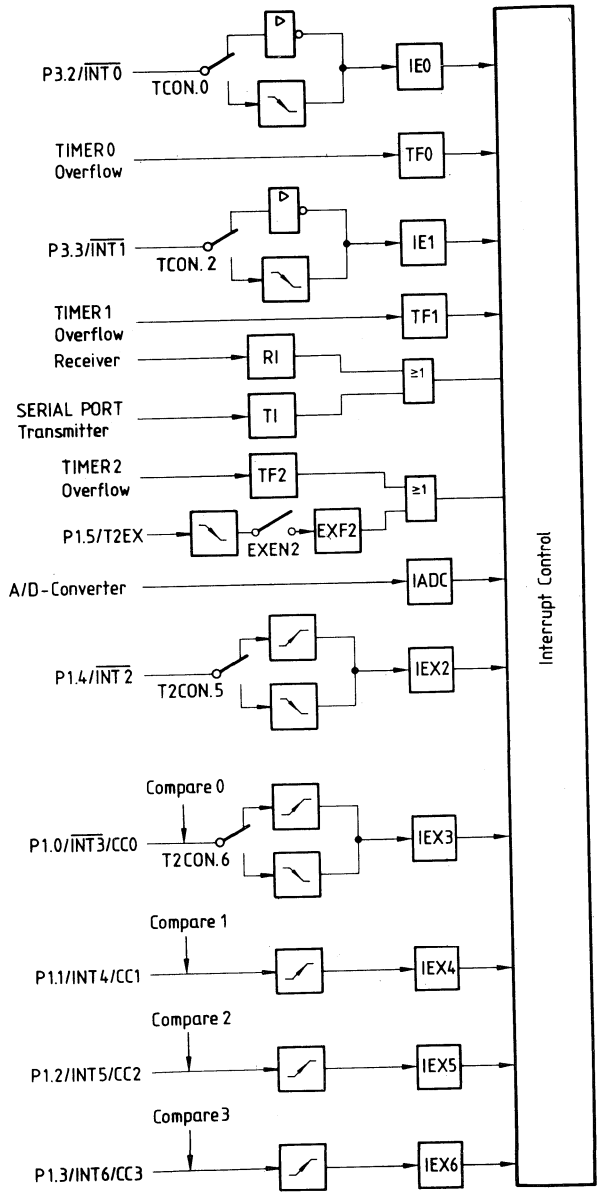
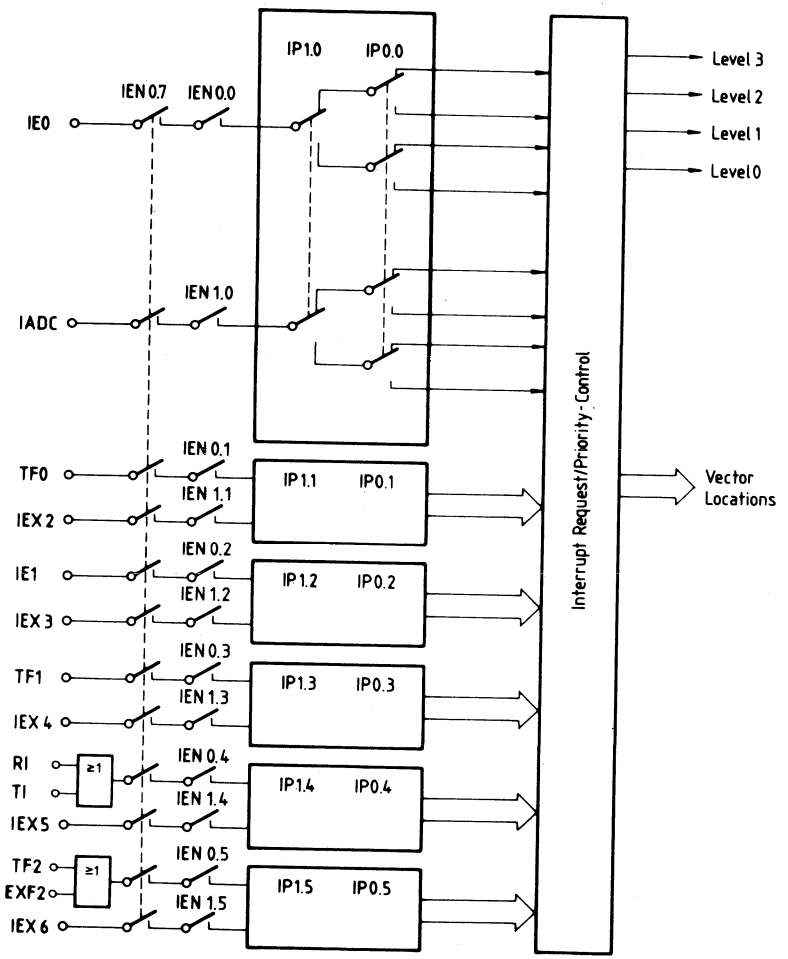


Figure 6
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped during active mode of the device. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor (see section "power saving modes" below). Therefore it is possible to use the idle mode in combination with the watchdog timer function. But even the watchdog timer cannot reset the device when one of the power saving modes is entered accidentally.
For these reasons several precautions are taken against unintentional entering of the power-down or idle mode (see below).

Power Saving Modes

The ACMOS technology of the SAB 80C515 allows two new power saving modes of the device: The idle mode and the power-down mode. These modes replace the power-down supply mode via pin VPD of the SAB 80515 (NMOS). The SAB 80C515 is supplied via pins V_{CC} also during idle and power-down operation.

However, there are applications where unintentional entering of these power saving modes must be absolutely avoided. Such critical applications often use the watchdog timer to prevent the system from program upsets. Then accidental entering of the power saving modes would even stop the watchdog timer and would circumvent the watchdog timer's task of system protection.

Thus, the SAB 80C515 has an extra pin that allows it to disable both of the power saving modes. When pin $\overline{PE}$ is held high, idle mode and power-down mode are completely disabled and the instruction sequences that are used for entering these modes (see below) will NOT affect the normal operation of the device. When $\overline{PE}$ is held low, the use of the idle mode and of power-down mode is possible as described in the following sections.

Pin $\overline{PE}$ has a weak internal pullup resistor. Thus, when left open, the power saving modes are disabled.

The Special Function Register PCON

In the NMOS version SAB 80515 the SFR PCON (address 87H) contains only bit SMOD; in the CMOS version SAB 80C515 there are more bits used (see table 3).

The bits PDE, PDS and IDLE, IDLS select the power-down mode or the idle mode, respectively, when the use of the power saving modes is enabled by pin $\overline{PE}$ (see below). If the power-down mode and the idle mode are set at the same time, power-down takes precedence.

Furthermore, register PCON contains two general purpose flags. For example, the flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. Then an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The reset value of PCON is 000X0000B.

Table 3
SFR PCON (87H)

SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE	87H
7	6	5	4	3	2	1	0	

Symbol	Position	Function
SMOD	PCON.7	When set, the baud rate of the serial channel in mode 1, 2, 3 is doubled.
PDS	PCON.6	Power-down start bit. The instruction that sets the PDS flag bit is the last instruction before entering the power-down mode.
IDLS	PCON.5	Idle start bit. The instruction that sets the IDLS flag bit is the last instruction before entering the idle mode.
–	PCON.4	Reserved
GF1	PCON.3	General purpose flag
GF0	PCON.2	General purpose flag
PDE	PCON.1	Power-down enable bit. When set, starting of the power-down mode is enabled.
IDLE	PCON.0	Idle mode enable bit. When set, starting of the idle mode is enabled.

Idle Mode

In the idle mode the oscillator of the SAB 80C515 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, and all timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.

The reduction of power consumption, which can be achieved by this feature depends on the number of peripherals running.

If all timers are stopped and the A/D converter and the serial interface are not running, the maximum power reduction can be achieved. This state is also the test condition for the idle mode I_{CC} (see DC characteristics, note 5).

So the user has to take care which peripheral should continue to run and which has to be stopped during idle mode. Also the state of all port pins – either the pins controlled by their latches or controlled by their secondary functions – depends on the status of the controller when entering idle mode.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. This applies to the compare outputs as well as to the clock output signal or to the serial interface in case it cannot finish reception or transmission during normal operation. The control signals ALE and $\overline{\text{PSEN}}$ hold at logic high levles (see table 4).

Table 4
Status of External Pins during Idle and Power-Down Modes

Outputs	Last instruction executed from internal code memory		Last instruction executed from external code memory	
	Idle	Power-down	Idle	Power-down
ALE	HIGH	LOW	HIGH	LOW
PSEN	HIGH	LOW	HIGH	LOW
PORT 0	DATA	DATA	FLOAT	FLOAT
PORT 1	DATA/ALTER-NATE OUTPUTS	DATA/LAST OUTPUT	DATA/ALTER-NATE OUTPUTS	DATA/LAST OUTPUT
PORT 2	DATA	DATA	ADDRESS	DATA
PORT 3	DATA/ALTER-NATE OUTPUTS	DATA/LAST OUTPUT	DATA/ALTER-NATE OUTPUTS	DATA/LAST OUTPUT
PORT 4	DATA	DATA	DATA	DATA
PORT 5	DATA	DATA	DATA	DATA

As in normal operation mode, the ports can be used as inputs during idle mode. Thus a capture or reload operation can be triggered, the timers can be used to count external events, and external interrupts will be detected.

The idle mode is a useful feature which makes it possible to "freeze" the processor's status – either for a pre-defined time, or until an external event reverts the controller to normal operation, as discussed below. The watchdog timer is the only peripheral which is automatically stopped during idle mode. If it were not disabled on entering idle mode, the watchdog timer would reset the controller, thus abandoning the idle mode.

When idle mode is used, pin $\overline{PE}$ must be held on low level. The idle mode is then entered by two consecutive instructions. The first instruction sets the flag bit IDLE (PCON.0) and must not set bit IDLS (PCON.5), the following instruction sets the start bit IDLS (PCON.5) and must not set bit IDLE (PCON.0). The hardware ensures that a concurrent setting of both bits, IDLE and IDLS, does not initiate the idle mode. Bits IDLE and IDLS will automatically be cleared after being set. If one of these register bits is read the value that appears is 0 (see table 3). This double instruction is implemented to minimize the chance of an unintentional entering of the idle mode which would leave the watchdog timer's task of system protection without effect.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the idle mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL   PCON,00000001B   ;Set bit IDLE, bit IDLS
                       must not be set
ORL   PCON,00100000B   ;Set bit IDLS, bit IDLE
                       must not be set
```

The instruction that sets bit IDLS is the last instruction executed before going into idle mode.

There are tow ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Power-Down Mode

In the power-down mode, the on-chip oscillator is stopped. Therefore all functions are stopped; only the contents of the on-chip RAM and the SFR's are maintained. The port pins controlled by their port latches output the values that are held by their SFR's. The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power-down mode; when the clockout signal (CLKOUT, P1.6) is enabled, it will stop at low level. ALE and $\overline{PSEN}$ hold at logic low level (see table 4).

To enter the power-down mode the pin $\overline{PE}$ must be on low level. The power-down mode then is entered by two consecutive instructions. The first instruction has to set the flag bit PDE (PCON.1) and must not set bit PDS (PCON.6), the following instruction has to set the start bit PDS (PCON.6) and must not set bit PDE (PCON.1). The hardware ensures that a concurrent setting of both bits, PDE and PDS, does not initiate the power-down mode. Bits PDE and PDS will automatically be cleared after having been set and the value shown by reading one of these bits is always 0 (see table 3). This double instruction is implemented to minimize the chance of unintentionally entering the power-down mode which could possibly "freeze" the chip's activity in an undesired status.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the power-down mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL   PCON,00000010B   ;Set bit PDE, bit PDS
                       must not be set
ORL   PCON,01000000B   ;Set bit PDS, bit PDE
                       must not be set
```

The instruction that sets bit PDS is the last instruction executed before going into power-down mode.

The only exit from power-down mode is a hardware reset. Reset will redefine all SFR's, but will not change the contents of the internal RAM.

In the power-down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power-down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power-down mode is terminated. The reset signal that terminates the power-down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Differences in Pin Assignments of the SAB 80C515 and SAB 80515

Since the SAB 80C515 is designed in CMOS technology, this device requires no V_{BB} pin, because the die's substrate is internally connected to V_{CC}.

Furthermore, the RAM backup power supply via pin V_{PD} is replaced by the software-controlled power-down mode and power supply via V_{CC}.

Therefore, pins V_{BB} and V_{PD} of the NMOS version SAB 80515 are used for other functions in the SAB 80C515.

Pin 4 (the former pin V_{PD}) is the new $\overline{PE}$ pin which enables the use of the power saving modes.

Pin 37 (the former pin V_{BB}) becomes an additional V_{CC} pin. Thus, it is possible to insert a decoupling capacitor between pin 37 (V_{CC}) and pin 38 (V_{SS}) very close to the device, thereby avoiding long wiring and reducing the voltage distortion resulting from high dynamic current peaks.

There is a a difference between the NMOS and CMOS version concerning the clock circuitry. When the device is driven from an external source, pin XTAL 2 must be driven by the clock signal; pin XTAL 1, however, must be left be open in the SAB 80C515 (must be tied low in the NMOS version). When using the oscillator with a crystal there is no difference in the circuitry.

Thus, due to its pin compatibility the SAB 80C515 normally substitutes any SAB 80515 without redesign of the user's printed circuit board; but the user has to take care that the two V_{CC} pins are hardwired on chip. In any case, it is recommended that power is supplied on both V_{CC} pins of the SAB 80C515 to improve the power supply to the chip. If the power saving modes are to be used, pin $\overline{PE}$ must be tied low, otherwise these modes are disabled.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex code	Number of bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A, ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70°C for the SAB 80C515
	−40 to + 85°C for SAB 80C515-T40/85
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to V_{CC} + 0.5 V
Voltage on V_{CC} to V_{SS}	−0.5 to + 6.5 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ±20%; V_{SS} = 0 V;
T_A = 0 to +70°C for SAB 80C515/80C535
T_A = −40 to +85°C for SAB 80C515/80C535-T40/85

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$)	V_{IL}	−0.5	$0.2V_{CC}-0.1$	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	−0.5	$0.2V_{CC}-0.3$	V	–
Input high voltage (except $\overline{RESET}$ and XTAL2)	V_{IH}	2.0 V_{CC} +0.9	V_{CC}+0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC}+0.5	V	–
Input high voltage to $\overline{RESET}$	V_{IH2}	0.6 V_{CC}	V_{CC}+0.5	V	–
Output low voltage, ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage, port 0, ALE, $\overline{PSEN}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage, ports 1, 2, 3, 4, 5	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = −80 µA V_{CC} = 5 V ±10% I_{OH} = −10 µA
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = −400 µA, V_{CC} = 5 V±10% I_{OH} = −40 µA [2]
Logic 0 input current, ports 1, 2, 3, 4, 5	I_{IL}	–	−50	µA	V_{IN} = 0.45 V
Input low current to $\overline{RESET}$ for reset	I_{IL2}	–	−100	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	I_{TL}	–	−650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	±10	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25°C
Power-down current	I_{PD}	–	50	µA	V_{CC} = 2 V to 6 V [3]

Maximum I_{CC} (mA)

		Active Mode [4]			Idle Mode [5]		
Frequency	V_{CC}	4 V	5 V	6 V	4 V	5 V	6 V
0.5 MHz		TBD	TBD	TBD	TBD	TBD	TBD
3.5 MHz		TBD	TBD	TBD	TBD	TBD	TBD
8.0 MHz		TBD	TBD	TBD	TBD	TBD	TBD
12 MHz		TBD	45	TBD	TBD	10	TBD

Note [1]: Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. Then, it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmit-trigger strobe input.

Note [2]: Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

Note [3]: Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = Port 6 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS}; $\overline{RESET}$ = V_{CC}; all other pins are disconnected.

Note [4]: I_{CC} (active mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; $\overline{EA}$ = Port 0 = Port 6 = V_{CC}; $\overline{RESET}$ = V_{SS}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

Note [5]: I_{CC} (idle mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = V_{CC}; $\overline{RESET}$ = V_{CC}; all other pins are disconnected; all on-chip peripherals are disabled.

A/D Converter Characteristics

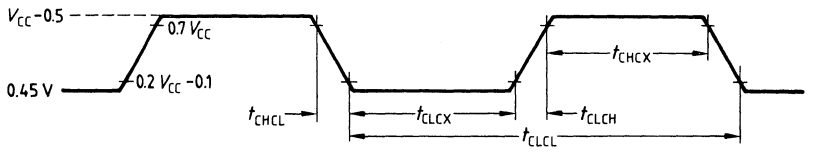
V_{CC} – 5 V ±20%; V_{SS} = 0 V; V_{AREF} = V_{CC} ±5%; V_{AGND} = V_{SS} ±0.2 V; $V_{IntAREF}$ - $V_{IntAGND}$ ≥ 1 V
T_A = 0 to + 70°C for SAB 80C515/80C535
T_A = −40 to +85°C for SAB 80C515/80C535-T40/85

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND}− 0.2	–	V_{AREF} + 0.2	V	–
Analog input capacitance	C_I	–	25	–	pF	[6]
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	5 t_{CY}	µs	–	
Conversion time (inc. sample time)	t_C	–	–	14 t_{CY}	µs	–
Differential non-linearity	DNLE	–	±1/2	±1	LSB	$V_{IntAREF}$ =
Integral non-linearity	INLE	–	±1/2	±1	LSB	V_{AREF} = V_{CC}
Offset error			±1/2	±1	LSB	$V_{IntAGND}$ =
Gain error			±1/2	±1	LSB	V_{AGND} = V_{SS}
Total unadjusted error	TUE		±1	±2	LSB	[6]
V_{AREF} supply current	I_{REF}	–	–	5	mA	[7]
Internal reference error	$V_{IntREFERR}$	–	–	TBD	mV	[7]

Note [6]: The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

Note [7]: The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode
t_{CLCH} = t_{CHCL} = 5 ns



AC Characteristics

V_{CC} = 5 V ±20%; V_{SS} = 0 V
(C_L for Port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all outputs = 80 pF)
T_A = 0 to +70°C for SAB 80C515/80C535
T_A = −40 to +85°C for SAB 80C515/80C535-T40/85

Program Memory Characteristics

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2\,t_{CLCL}$-40	–	ns
Address setup to ALE	t_{AVLL}	53	–	t_{CLCL}-30	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL}-35	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	$4\,t_{CLCL}$-100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	t_{CLCL}-25	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3\,t_{CLCL}$-35	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3\,t_{CLCL}$-100	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	63	–	t_{CLCL}-20	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	75	–	t_{CLCL}-8	–	ns
Address to valid instruction in	t_{AVIV}	–	302	–	$5\,t_{CLCL}$-115	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB 80C515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

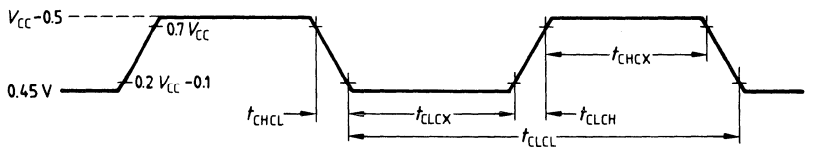
External Data Memory Characteristics

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6\,t_{CLCL}$-100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6\,t_{CLCL}$-100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2\,t_{CLCL}$-35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5\,t_{CLCL}$-165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2\,t_{CLCL}$-70	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8\,t_{CLCL}$-150	ns
Address to valid data in	t_{AVDV}	–	585	–	$9\,t_{CLCL}$-165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	$4\,t_{CLCL}$-130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	t_{CLCL}-50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7\,t_{CLCL}$-150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL}-50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

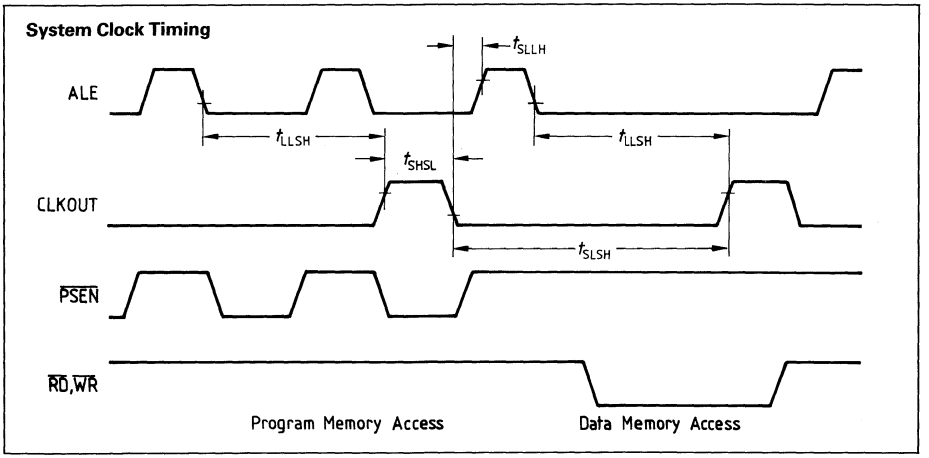
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 0.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	2000	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	12	MHz
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

External Clock Cycle



System Clock Timing

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE to CLKOUT	t_{LLSH}	543	–	$7\,t_{CLCL}$-40	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2\,t_{CLCL}$-40	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10\,t_{CLCL}$-40	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	t_{CLCL}-40	t_{CLCL}+40	ns

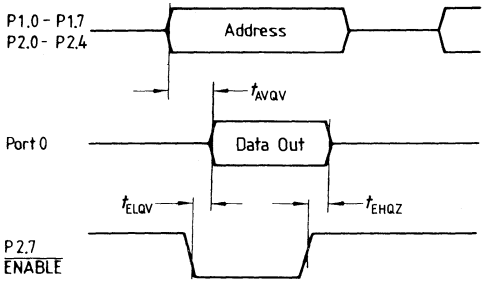


ROM Verification Characteristics

T_A = 25°C ±5°C; V_{CC} = 5V ±20%; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification

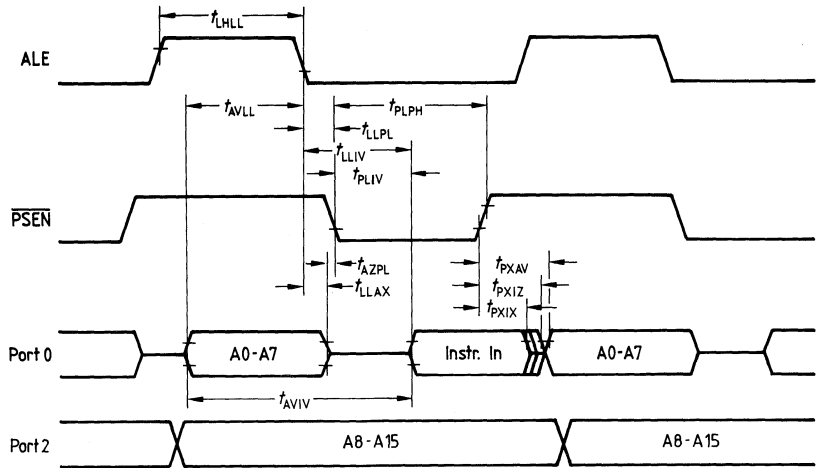


Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12
Data: Port 0 = D0–D7

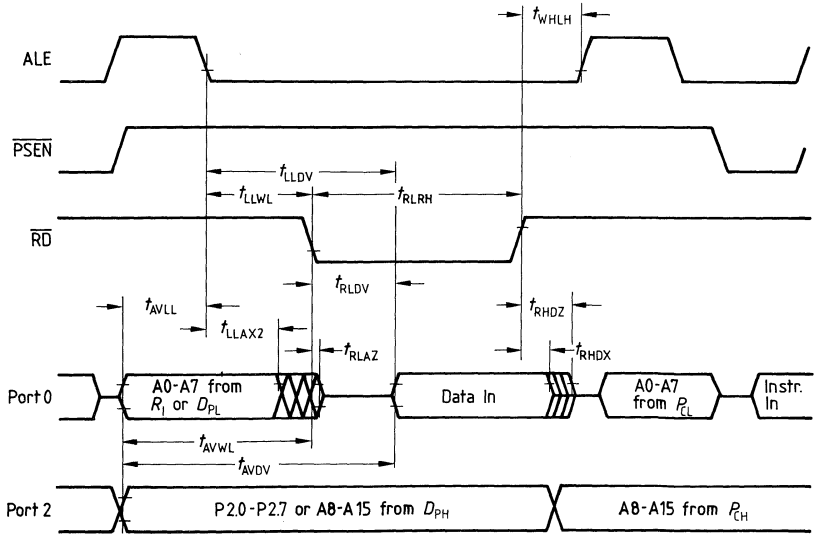
Inputs: P2.5–P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

Waveforms

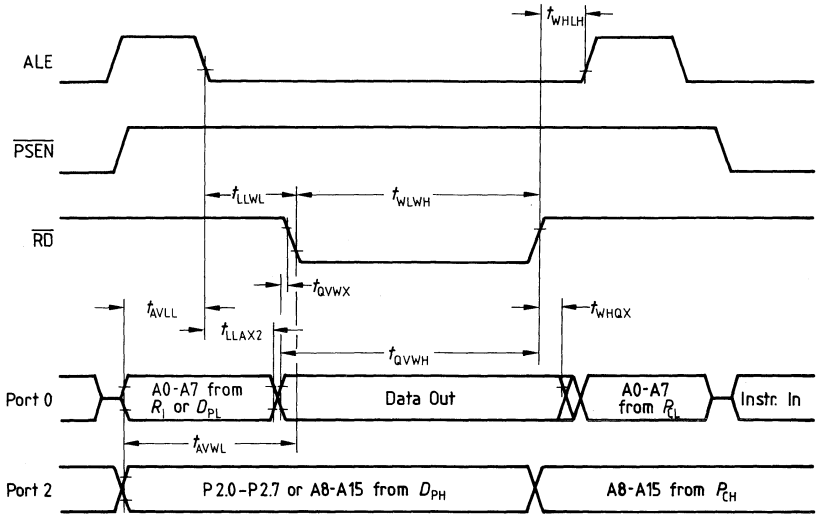
Program Memory Read Cycle



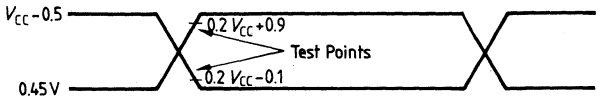
Data Memory Read Cycle



Data Memory Write Cycle

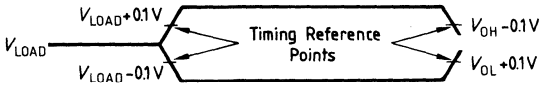


AC Testing: Input, Output Waveforms



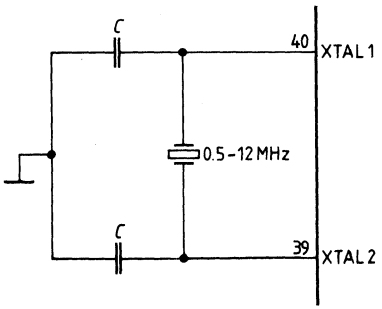
AC Inputs during testing are driven at V_{CC} −0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Float Waveforms

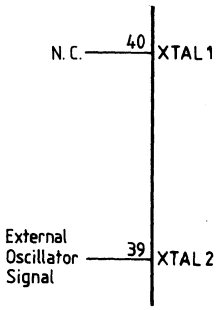


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV deviation from the load voltage V_{OH}/V_{OL} occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Recommended Oscillator Circuits



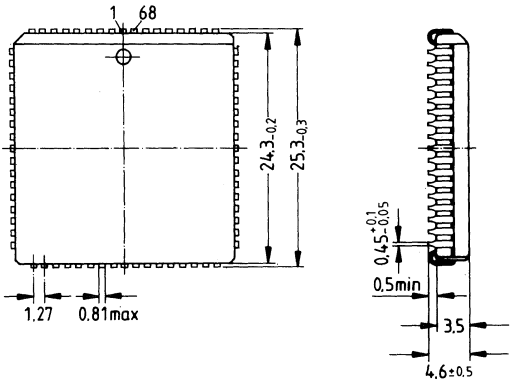
C = 30 pF ± 10 pF
(incl. stray capacitance)
Crystal Oscillator Mode



Driving from External Source

Package Outline

68-Pin Plastic Leaded Chip Carrier Package, PL-CC-68



Dimensions in mm

Ordering Information

Type	Ordering code	Description
		8-bit CMOS microcontroller
SAB 80C515-N	Q 67120-C297	with mask-programmable ROM (plastic)
SAB 80C535-N	Q 67120-C366	for external memory (plastic)
SAB 80C515-N-T40/85	Q 67120-C388	with mask-programmable ROM (plastic), ext. temperature
SAB 80C535-N-T40/85	Q 67120-C387	for external memory (plastic), ext. temperature

8-Bit Single-Chip Microcontrollers
Extended Temperature Range

Preliminary

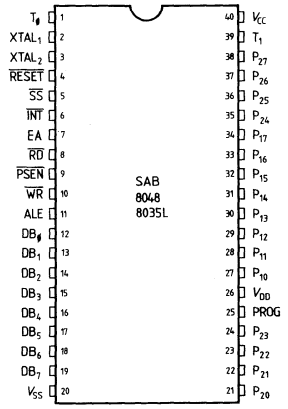
SAB 8035/8048
8 Bit Single Chip Microcontroller

Extended Temperature Range: −40 to + 85°C
−40 to +110°C

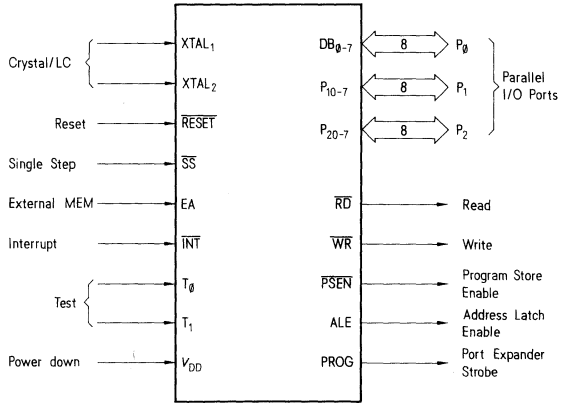
SAB 8048-P-T40/85	**Mask Programmable ROM**
SAB 8048-P-T40/110	**Mask Programmable ROM**
SAB 8035L-P-T40/85	**External ROM**

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- 8-Bit Internal Timer/Event Counter
- Instructions 1 or 2 Cycles, 2.5 µs or 5.0 µs Cycle Time
- 96 Instructions: 70% Single Byte
- Compatible with SAB 8080/8085 Peripherals
- 1K×8 ROM
  64×8 RAM
  27 I/O Lines
- 2 Single Level Interrupts: Internal Timer/Counter and External
- Single 5V Supply
- Power Down Mode: Standby Current for Internal RAM 15mA

Pin Configuration



Logic Symbol



The SAB 8048/8035L are 8-Bit Single-Chip-Microcontroller implemented in +5 Volts, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40 pin package. It is 100% compatible with the industry standard 8048.

The SAB 8048 contains a 1K×8 program memory, a 64×8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the SAB 8048 can be expanded using standard memories and SAB 8080/8085 peripherals. The SAB 8035L is the equivalent of an SAB 8048 without program memory and can be used with external ROM and RAM.

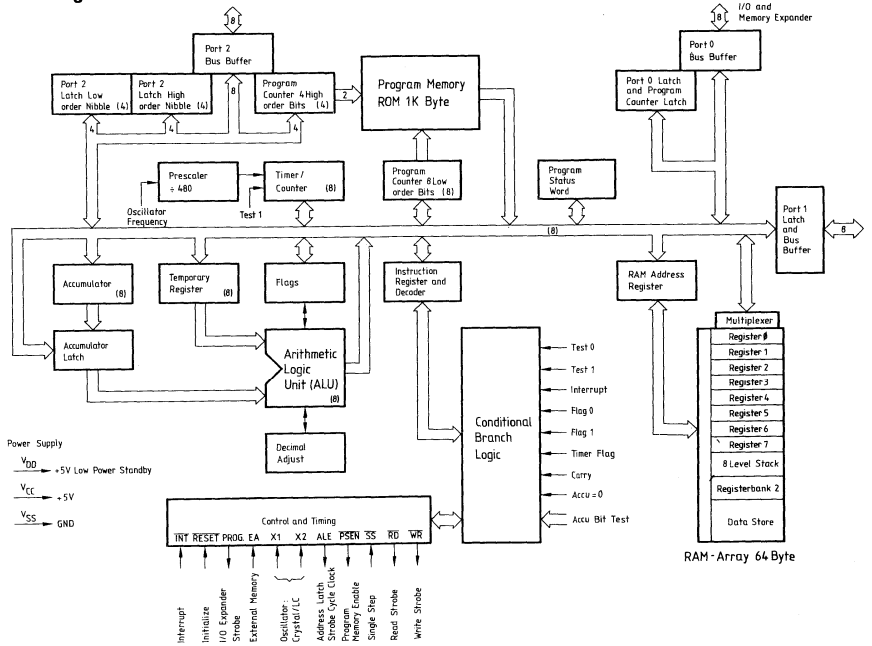
These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from a instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

Pin Description

Symbol	Pin No.	I/O	Function
$T_\emptyset$	1	I/O	Input pin testable using the conditional transfer instructions JT$\emptyset$ and JNT$\emptyset$. $T_\emptyset$ can be designated as a clock output using ENT$\emptyset$ CLK instruction
$XTAL_1$, $XTAL_2$	2,3		Inputs for internal oscillator with crystal or external source (non TTL VIH)
$\overline{RESET}$	4	I	Input which is used to initialize the processor (Activ low). Also used during power down (non TTL VIH)
$\overline{SS}$	5	I	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (active low)
$\overline{INT}$	6	I	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (aktive low)
EA	7	I	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (active high)
$\overline{RD}$	8	O	Output strobe activated during a BUS read. Can be used to enable data on the bus from an external device. Used as a read strobe to external data memory (active low)
$\overline{PSEN}$	9	O	Program store enable. This output occurs only during a fetch to external program memory (active low)
$\overline{WR}$	10	O	Output strobe during a bus write (active low). Used as a write strobe to external data memory
ALE	11	O	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory
$DB_\emptyset$–DB_7	12-19	I/O	Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$

Symbol	Pin No.	I/O	Function
P_{20}–P_{27}	21-24 35-38	I/O	8-Bit quasi-bidirectional I/O-Port. P_{20}–P_{23} contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for SAB 8243
PROG	25	O	Output strobe for SAB 8243 I/O expander
P_{10}–P_{17}	27-34	I/O	8-Bit quasi-bidirectional I/O-Port.
T_1	39	I	Input pin testable using the JT1 and JTN1 instructions. Can be designated the timer/counter input using the STRT CNT instruction
V_{CC}	40		5V Main power supply
V_{DD}	26		5V Power Down Voltage
V_{SS}	20		GND potential

Block Diagram



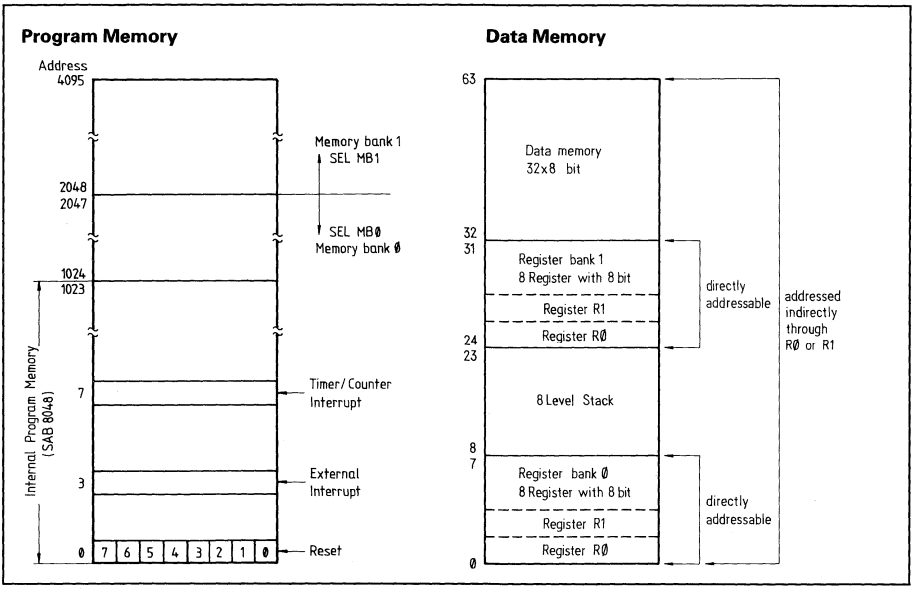
Functional Description

Program Memory

Program memory of SAB 8048 consists of 1024 words 8-bit wide which are adressed by the program counter. Program memory can be used to store constants as well as program instructions. Three locations in Program Memory are reserved to service the two Interrupts (Timer/Counter and external) and the Reset.

Data Memory

Data memory of SAB 8048 is organized as 64 words, 8-bits wide containing the stack and 2 register banks of 8 directly addressable registers.



Timer/Counter

The internal 8-bit binary up-counter can be used to count external events and to generate accurate time delays. The increment from maximum count FF to 00 (overflow) results in the setting of an overflow flag flip-flop and in the generation of interrupt request if the interrupt is enabled.

Depending upon the type of START-Instruction used the timer/counter is clocked by the oscillator frequency: 480 or an external clock.

The timer/counter is presettable and readable with two MOV instructions.

Interrupts

The two interrupts (timer/counter an external) have the same priority. They can be enabled or disabled under program control.

Input/Output

The SAB 8048 has 27 lines which can be used for I/O functions. These lines are grouped as three 8-bit ports and three test inputs.

Port 1 and 2 are called quasi-bidirectional because each line can serve as an input, an output, or both. Port 0 is a true bidirectional port with associated input and output strobes. Input and output lines on this port cannot be mixed however.

With 4 control and strobe lines, port 0 can be used as a bidirectional bus port to interface external memory and I/O devices. The three pins T0, T1, and $\overline{INT}$ serve as inputs and are testable with conditional jump instructions.

Symbols and Abbreviations used

A	Accumulator
AC	Auxillary Carry
Adr	12-Bit Program Memory Address
An	Accumulator Bit n
BS	Bank Switch
BUS	Bus Port
CY	Carry
CLK	Clock
CNT	Event Counter
Data	8-Bit Number or Expression
DBF	Memory Bank Flip-Flop
FØ, F1	Flag Ø, 1
$\overline{INT}$	Interrupt
PC	Program Counter
PCn	Program Counter Bit n
Pp	Port 4–7 (for I/O-Extension with SAB 8243)
Pr	Port 1 or Port 2
PSW	Program Status Word
Rn	Register Bit n
Rr	Register Ø–7
SP	Stackpointer
T	Timer
TF	Timer Flag
TØ, T1	Test Ø, Test 1
X	Mnemonic for External RAM
#	Immediate Data Prefix
@	Indirect Address Prefix
Page	Memory Block of 256 Byte
( )	Content
→	is moved to
↔	is exchanged with
∧	logical UND
∨	logical OR
⊻	logical EXCLUSIV OR
–	Complement

Instruction Set

Mnemonic	Function	Description	Hex Code	Flag	Bytes	Cycles
Accumulator and Register Move Instructions						
MOV A, Rr	(Rr) → A	Move Register Contents	F8–FF		1	1
MOV A, @ Rr	((Rr)) → A	Move Data Memory Contents to Accumulator	FØ–F1		1	1
MOV A, # Data	Data → A	Move Immediate Data Data to Accumulator	23		2	2
MOV A, PSW	(PSW) → A	Move PSW Contents to Accumulator	C7		1	1
MOV PSW, A	(A) → PSW	Move Accumulator Contents to PSW	D7	CY, AC	1	1
MOV Rr, A	(A) → Rr	Move AccumulatorContents to Register	A8–AF		1	1
MOV @ Rr, A	(A) → (Rr)	Move Accumulator Contents to Data Memory	AØ–A1		1	1
MOV Rr, # Data	Data → Rr	Move Immediate Data to Register	B8–BF		2	2
MOV @ Rr, # Data	Data → (Rr)	Move Immediate Data to Data Memory	BØ–B1		2	2
MOVX A, @ Rr	((Rr)) → A	Move External-Data-Memory Contents to Accumulator	8Ø–81		1	2
MOVX @ Rr, A	(A) → (Rr)	Move Accumulator Contents to External Data Memory	9Ø–91		1	2
XCH A, Rr	(Rr) ↔ (A)	Exchange Accumulator and Register Contents	28–2F		1	1
XCH A, @ Rr	((Rr)) ↔ (A)	Exchange Accumulator and Data Memory Contents	2Ø–21		1	1
XCHD A, @ Rr	$((Rr))_{Ø-3} \leftrightarrow (A)_{Ø-3}$	Exchange Accumulator and Data Memory 4-Bit Data	3Ø–31		1	1
MOVP3 A, @ A	(PC) save $(A) \rightarrow PC_{Ø-7}$ $011 \rightarrow PC_{8-11}$ ((PC)) → A PC restor	Move Page 3 Data to Accumulator	E3		1	2
MOVP A, @ A	(PC) save $(A) \rightarrow PC_{Ø-7}$ ((PC)) → A PC restor	Move Current Page Data to Accumulator	A3		1	2
SWAP A	$(A)_{Ø-3} \leftrightarrow (A)_{4-7}$	Swap Nibble within Accumulator	47		1	1
Timer/Counter Move Instructions						
MOV A, T	(T) → A	Move Timer/Counter Contents to Accumulator	42		1	1
MOV T, A	(A) → T	Move Accumulator Contents to Timer/Counter	62		1	1

Mnemonic	Function	Description	Hex Code	Flag	Bytes	Cycles
Port Move Instructions						
IN A, Pr	(Pr) → A	Input Port 1 or 2 Data to Accumulator	Ø9–ØA		1	2
OUTL Pr, A	(A) → Pr	Output Accumulator Data to Port 1 or 2	39–3A		1	2
ANL Pr, # Data	(Pr) ∧ Data → Pr	Logical AND Port 1–2 with Immediate Mask	99–9A		2	2
ORL Pr, # Data	(Pr) ∨ Data → Pr	Logical OR Port 1–2 with Immediate Mask	89–8A		2	2
INS A, BUS	(BUS) → A	Strobed Input of BUS-Data to Accumulator	Ø8		1	2
OUTL BUS, A	(A) → BUS	Output Accumulator Data to BUS	Ø2		1	2
ANL BUS, # Data	(BUS) ∧ Data → BUS	Logical AND BUS with Immediate Mask	98		2	2
ORL BUS, # Data	(BUS) ∨ Data → BUS	Logical OR BUS with Immediate Mask	88		2	2
MOVD A, P_P	$(P_P) \rightarrow A_{Ø-3}$ $Ø \rightarrow A_{4-7}$	Move Port 4–7 of SAB 8243 to Accumulator Port 4 5 6 7	ØC ØD ØE ØF		1 1 1 1	2 2 2 2
MOVD P_p, A	$(A)_{Ø-3} \rightarrow P_p$	Move Accumulator to Port 4–7 of SAB 8243 Port 4 5 6 7	3C 3D 3E 3F		1 1 1 1	2 2 2 2
ANLD P_p, A	$(A)_{Ø-3} \wedge (P_p) \rightarrow P_p$	Logical AND Port 4–7 of SAB 8243 with Accumulator Mask Port 4 5 6 7	9C 9D 9E 9F		1 1 1 1	2 2 2 2
ORLD P_P, A	$(A)_{Ø-3} \vee (P_P) \rightarrow P_P$	Logical OR Port 4–7 of SAB 8243 with Accumulator Mask Port 4 5 6 7	8C 8D 8E 8F		1 1 1 1	2 2 2 2
Arithmetic Accumulator Instructions						
ADD A, R_r	$(A)+(R_r) \rightarrow A$	Add Register Contents to Accumulator	68–6F	AC, CY	1	1
ADD A, @ R_r	$(A)+((R_r)) \rightarrow A$	Add Data Memory Contents to Accumulator	60 61	AC, CY	1	1
ADD A, # Data	(A)+Data → A	Add Immediate Data to Accumulator	Ø3	AC, CY	2	2
ADDC A, R_r	$(A)+(R_r)+(CY) \rightarrow A$	Add Carry and Register Contents to Accumulator	78–7F	AC, CY	1	1
ADDC A, @ R_r	$(A)+((R_r))+(CY) \rightarrow A$	Add Carry and Data Memory Contents to Accumulator	70 71	AC, CY	1	1
ADDC A, # Data	(A)+Data+(CY) → A	Add Carry and Immediate Data to Accumulator	13	AC, CY	2	2

Mnemonic		Function	Description	Hex Code	Flag	Bytes	Cycles
INC	A	(A)+1 → A	Increment Accumulator	17		1	1
DEC	A	(A)−1 → A	Decrement Accumulator	Ø7		1	1
DA	A		Decimal Adjust Accumulator	57	AC, CY	1	1

Arithmetic Register Instructions

INC	R_r	$(R_r)+1 \rightarrow R_r$	Increment Register	18−1F		1	1
DEC	R_r	$(R_r)-1 \rightarrow R_r$	Decrement Register	C8−CF		1	1
INC	@ R_r	$((R_r))+1 \rightarrow (R_r)$	Increment Data Memory Location	1Ø−11		1	1
DJNZ	R_r, Adr	$(R_r)-1 \rightarrow R_r$ if $(R_r) \neq Ø$ Adr → $PC_{Ø-7}$	Decrement Register and Test Register if Zero	E8−EF		2	2

Logical Accumulator and Register Instructions

ANL	A, R_r	$(A) \wedge (R_r) \rightarrow A$	Logical AND Accumulator with Register Mask	58−5F		1	1
ANL	A, @ R_r	$(A) \wedge ((R_r)) \rightarrow A$	Logical AND Accumulator with Memory Mask	5Ø 51		1	1
ANL	A, # Data	(A) ∧ Data → A	Logical AND Accumulator with Immediate Mask	53		2	2
ORL	A, R_r	$(A) \vee (R_r) \rightarrow A$	Logical OR Accumulator with Register Mask	48−4F		1	1
ORL	A, @ R_r	$(A) \vee ((R_r)) \rightarrow A$	Logical OR Accumulator with Memory Mask	4Ø 41		1	1
ORL	A, # Data	(A) ∨ Data → A	Logical OR Accumulator with Immediate Mask	43		2	2
XRL	A, R_r	$(A) \veebar (R_r) \rightarrow A$	Logical XOR Accumulator with Register Mask	D8−DF		1	1
XRL	A, @ R_r	$(A) \veebar ((R_r)) \rightarrow A$	Logical XOR Accumulator with Memory Mask	DØ D1		1	1
XRL	A, # Data	(A) ⊻ Data → A	Logical XOR Accumulator with Immediate Mask	D3		2	2
CLR	A	Ø → A	Clear Accumulator	27		1	1
CPL	A	$(\overline{A}) \rightarrow A$	Complement Accumulator	37		1	1

Rotate Instructions

RL	A	(An) → An+1	Rotate Accumulator Left without Carry	E7		1	1
RLC	A	(An) → An+1 $(A_7) \rightarrow$ CY (CY) → $A_Ø$	Rotate Accumulator Left through Carry	F7	CY	1	1
RR	A	(An+1) → An	Rotate Accumulator Right without Carry	77		1	1
RRC	A	(An+1) → An $(A_Ø) \rightarrow$ CY (CY) → A_7	Rotate Accumulator Right through Carry	67	CY	1	1

Mnemonic		Function	Description	Hex Code	Flag	Bytes	Cycles
Flag Instructions							
CLR	C	$\emptyset \rightarrow CY$	Clear Carry Bit	97	CY	1	1
CPL	C	$(\overline{CY}) \rightarrow CY$	Complement Carry Bit	A7	CY	1	1
CLR	F$\emptyset$	$\emptyset \rightarrow F\emptyset$	Clear Flag$\emptyset$	85		1	1
CPL	F$\emptyset$	$(\overline{F\emptyset}) \rightarrow F\emptyset$	Complement Flag $\emptyset$	95		1	1
CLR	F1	$\emptyset \rightarrow F1$	Clear Flag 1	A5		1	1
CPL	F1	$(\overline{F1}) \rightarrow F1$	Complement Flag 1	B5		1	1
Branch Instructions							
JMP	Adr	$Adr_{\emptyset-7} \rightarrow PC_{\emptyset-7}$ $Adr_{8-10} \rightarrow PC_{8-10}$ $DBF \rightarrow PC_{11}$	Direct Jump within 2K-Block Page $\emptyset$ 1 2 3 4 5 6 7	$\emptyset$4 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
JMPP	@ A	$((A)) \rightarrow PC_{\emptyset-7}$	Indirect Jump within Page	B3		1	2
JC	Adr	If (CY) = 1 $Adr \rightarrow PC_{\emptyset-7}$	Jump if Carry is set	F6		2	2
JNC	Adr	If (CY) = $\emptyset$ $Adr \rightarrow PC_{\emptyset-7}$	Jump if Carry is not set	E6		2	2
JZ	Adr	If (A) = $\emptyset$ $Adr \rightarrow PC_{\emptyset-7}$	Jump if Accumulator is Zero	C6		2	2
JNZ	Adr	If (A) $\neq \emptyset$ $Adr \rightarrow PC_{\emptyset-7}$	Jump if Accumulator is not Zero	96		2	2
JT$\emptyset$	Adr	If T$\emptyset$ = 1 $Adr \rightarrow PC_{\emptyset-7}$	Jump if Test $\emptyset$ is High	36		2	2
JNT$\emptyset$	Adr	If T$\emptyset$ = $\emptyset$ $Adr \rightarrow PC_{\emptyset-7}$	Jump if Test $\emptyset$ is Low	26		2	2
JT1	Adr	If T1 = 1 $Adr \rightarrow PC_{\emptyset-7}$	Jump if Test 1 is High	56		2	2
JNT1	Adr	If T1 = $\emptyset$ $Adr \rightarrow PC_{\emptyset-7}$	Jump if Test 1 is Low	46		2	2
JF$\emptyset$	Adr	If F$\emptyset$ = 1 $Adr \rightarrow PC_{\emptyset-7}$	Jump if Flag $\emptyset$ is set	B6		2	2
JF1	Adr	If F1 = 1 $Adr \rightarrow PC_{\emptyset-7}$	Jump if Flag 1 is set	76		2	2
JTF	Adr	If TF = 1 $Adr \rightarrow PC_{\emptyset-7}$ $\emptyset \rightarrow TF$	Jump if Timer Flag is set	16	TF	2	2
JNI	Adr	If $\overline{INIT}$ = $\emptyset$ $Adr \rightarrow PC_{\emptyset-7}$	Jump if Interrupt input is Low	86		2	2

Mnemonic		Function	Description		Hex Code	Flag	Bytes	Cycles
JBn	Adr	If Bit n = 1 Adr → PC_{0-7}	Jump if Accumulator Bit n is set	n = Ø	12		2	2
				1	32		2	2
				2	52		2	2
				3	72		2	2
				4	92		2	2
				5	B2		2	2
				6	D2		2	2
				7	F2		2	2

Subroutine Instructions

CALL	Adr	(PC_{0-11},PSW) → (SP) (SP)+1 → SP Adr_{0-7} → PC_{0-7} Adr_{8-10} → PC_{8-10} DBF → PC_{11}	Subroutine Call	Page Ø	14		2	2
				1	34		2	2
				2	54		2	2
				3	74		2	2
				4	94		2	2
				5	B4		2	2
				6	D4		2	2
				7	F4		2	2
RET		(SP)−1 → SP ((SP)) → PC	Return without PSW Restore		83		1	2
RETR		(SP)−1 → SP ((SP)) → PC ((SP)) → PSW_{4-7}	Return with PSW Restore		93	AC, CY	1	2

Control Instructions

STRT	T		Start Timer	55		1	1
STRT	CNT		Start Event Counter	45		1	1
STOP	TCNT		Stop Timer/Event-Counter	65		1	1
EN	TCNTI		Enable Timer/Counter Interrupt	25		1	1
DIS	TCNTI		Disable Timer/Counter Interrupt	35		1	1
EN	I		Enable External Interrupt	Ø5		1	1
DIS	I		Disable External Interrupt	15		1	1
SEL	RBØ	Ø → BS	Select Register Bank Ø	C5		1	1
SEL	RB1	1 → BS	Select Register Bank 1	D5		1	1
SEL	MBØ	Ø → DBF	Select Memory Bank Ø	E5		1	1
SEL	MB1	1 → DBF	Select Memory Bank 1	F5		1	1
ENTØ	CLK		Enable Clock Output	75		1	1
NOP			The NOP Instruction	ØØ		1	1

Absolute Maximum Ratings[1)]

Ambient Temperature Under Bias	−40 to + 85°C for T40/85 −40 to +110°C for T40/110
Storage Temperature	−65 to +125°C
Voltage On Any Pin With Respect to Ground	−0.5 to + 7 V
Power Dissipation	1.5 W

D.C. and Operating Characteristics

$V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$; T_A −40 to + 85°C for T40/85
T_A −40 to +110°C for T40/110

Symbol	Parameter	Limit values			Unit	Test Conditions
		min.	typ.	max.		
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, XTAL1, XTAL2)	−0.5	–	0.8	V	–
V_{IL1}	Input Low Voltage ($\overline{RESET}$, XTAL1, XTAL2)	−0.5	–	0.6	V	–
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0	–	V_{CC}	V	–
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)	3.8	–	V_{CC}	V	–
V_{OL}	Output Low Voltage (BUS)	–	–	0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	–	–	0.45	V	I_{OL} = 1.8 mA
V_{OL2}	Output Low Voltage (PROG)	–	–	0.45	V	I_{OL} = 1.0 mA
V_{OL3}	Output Low Voltage (All Other Outputs)	–	–	0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (BUS)	2.4	–	–	V	I_{OH} = 400 µA
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4	–	–	V	I_{OH} = 100 µA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4	–	–	V	I_{OH} = 40 µA
I_{L1}	Input Leakage Current (T1, $\overline{INT}$)	–	–	±10	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LI1}	Input Leakage Current (P10–P17, P20–P27, EA, $\overline{SS}$)	–	–	−500	µA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)	–	–	±10	µA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current	–	5	15	mA	–
$I_{DD}+I_{CC}$	Total Supply Current	–	60	135	mA	–

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

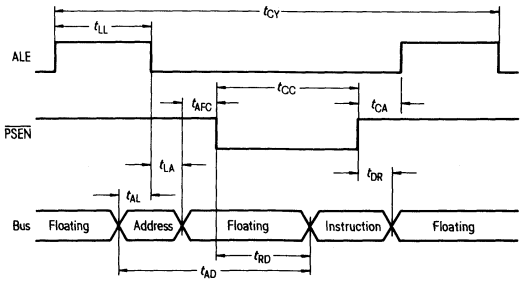
$V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$; T_A −40 to + 85°C for T40/85
T_A −40 to +110°C for T40/110

Symbol	Parameter	Limit Values		Unit	Test Conditions *
		min.	max.		
t_{LL}	ALE Pulse Width	400	–	ns	–
t_{AL}	Address Setup to ALE	120	–	ns	–
t_{LA}	Address Hold from ALE	80	–	ns	–
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700	–	ns	–
t_{DW}	Data Setup before $\overline{WR}$	500	–	ns	–
t_{WD}	Data Hold After $\overline{WR}$	120	–	ns	C_L = 20 pF
t_{CY}	Cycle Time	2.5	15.0	µs	6 MHz Crystal = 2.5 µs
t_{DR}	Data Hold	0	200	ns	–
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In	–	500	ns	–
t_{AW}	Address Setup to $\overline{WR}$	230	–	ns	–
t_{AD}	Address Setup to Data In	–	950	ns	–
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0	–	ns	–
t_{CA}	Control Pulse to ALE	10	–	ns	–

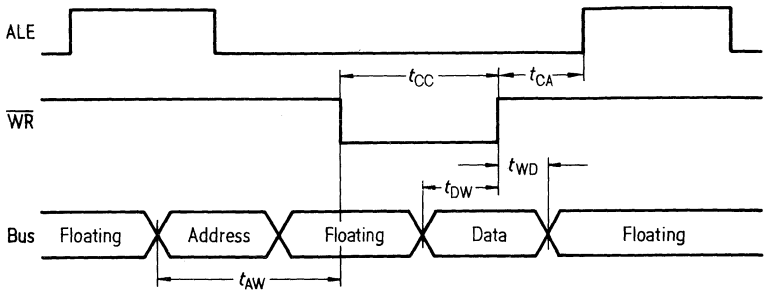
* Control outputs: C_L = 80 pF; BUS outputs: C_L = 150 pF

Waveforms

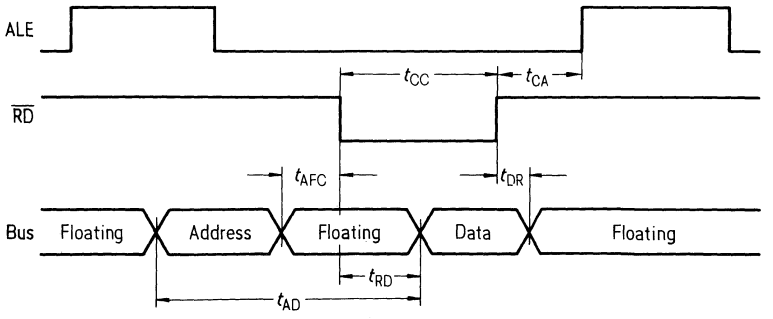
Instruction fetch from external program memory



Write to External Data Memory



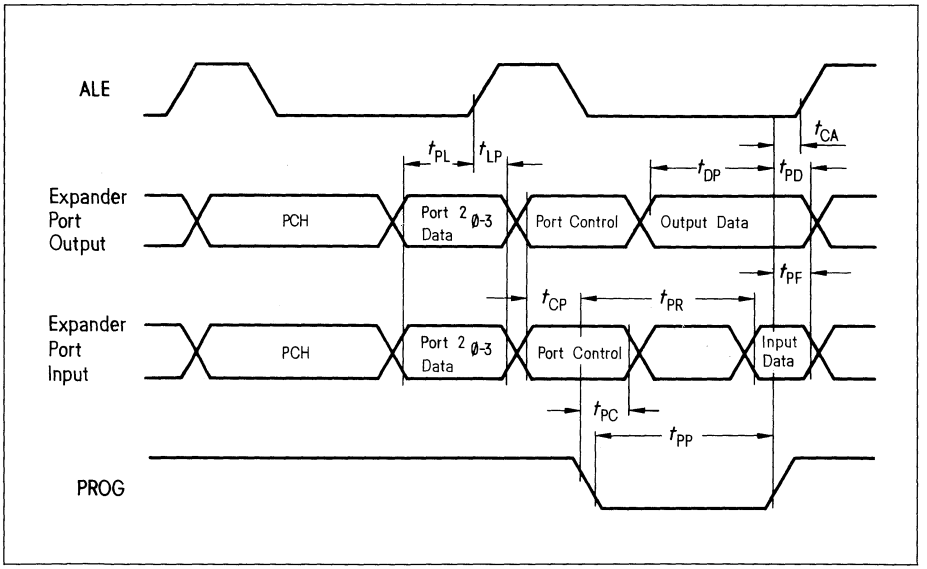
Read From External Data Memory



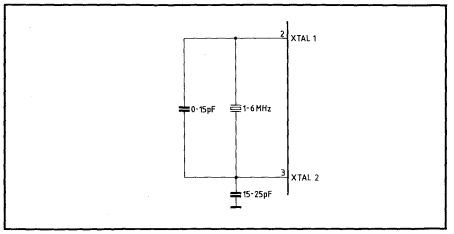
A.C. Characteristics (Port 2 Timing)

$V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$; T_A −40 to + 85°C for T40/85
T_A −40 to +110°C for T40/110

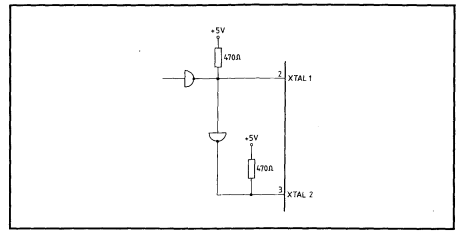
Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{CP}	Port Control Setup Before Falling Edge of PROG	110	–	ns
t_{PC}	Port Control Hold After Falling Edge of PROG	100	–	ns
t_{PR}	PROG to Time P2 Input Must Be Valid	–	810	ns
t_{PF}	Input Data Hold Time	0	150	ns
t_{DP}	Output Data Setup Time	250	–	ns
t_{PD}	Output Data Hold Time	65	–	ns
t_{PP}	PROG Pulse Width	1200	–	ns
t_{PL}	Port 2 I/O Data Setup	350	–	ns
t_{LP}	Port 2 I/O Data Hold	150	–	ns



Connecting the Oscillator Inputs



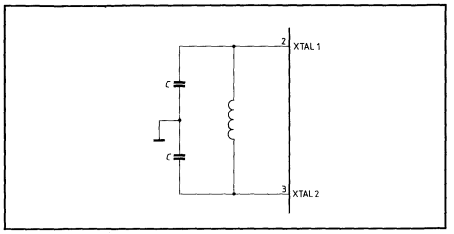
Crystal series resistance should be
$< 75\ \Omega$ at 6 MHz and $< 180\ \Omega$ at 3.6 MHz.



Both XTAL1 and XTAL2 should be driven.

Resistors to V_{CC} are needed to ensure $V_{IH} = 3.8$ V if TTL circuitry is used.

XTAL1 and XTAL2 must be high 35–65% of the period.

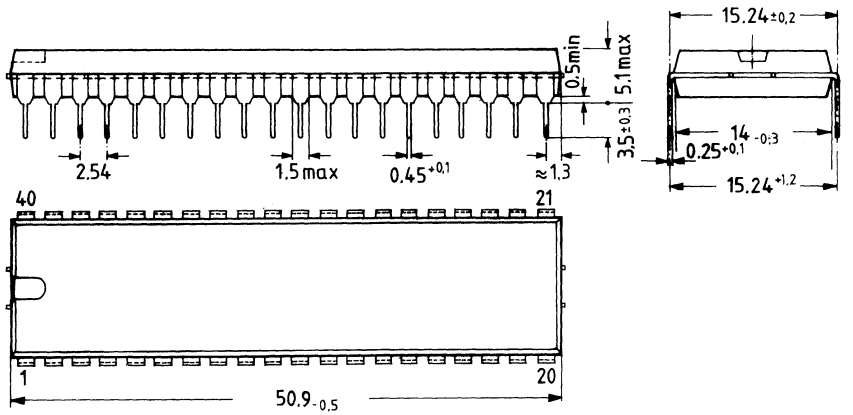


$$f = \frac{1}{2\pi\sqrt{LC'}} \qquad C' = \frac{C + 3\,C_{PP}}{2}$$

$C_{pp} \approx 5$–10 pF pin-to-pin capacitance

Package Outline

Plastic Package, P-DIP, 40 pins



Ordering Information

Type	Ordering code	Function
SAB 8048-P-T40/85	Q67120-C133	8 Bit Single-Chip-Microcomputer with maskprogrammable ROM (Plastic)
SAB 8048-P-T40/110	Q67120-C162	with maskprogrammable ROM (Plastic)
SAB 8035L-P-T40/85	Q67120-C140	with external ROM (Plastic)

Preliminary

SAB 8051A/8031A Ext.Temp. 8-Bit Single-Chip Microcontroller

Extended Temperature Range: −40 to + 85°C
−40 to +110°C

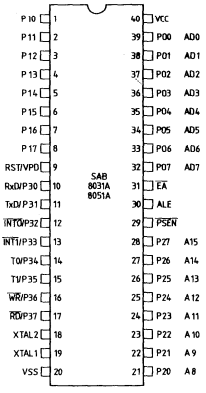
SAB 8051A-12-P-T40/85
SAB 8051A-10-P-T40/110 **Mask-Programmable ROM**

- Advanced version of the SAB 8031/8051 for extended temperature range
- SAB 8051A/8031A-12-T40/85: 12 MHz operation
- SAB 8051A/8031A-10-T40/110: 10 MHz operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines

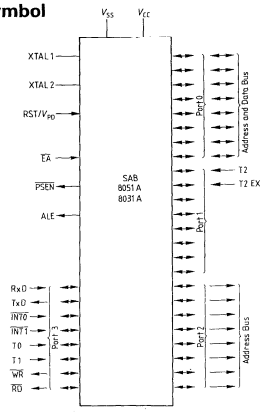
SAB 8031A-12-P-T40/85
SAB 8031A-10-P-T40/110 **External ROM**

- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable up to 128K
- Compatible with SAB 8080/8085 peripherals
- Boolean processor •
- 218 user bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide

Pin Configuration



Logic Symbol



The SAB 8051A/8031A for the two extended temperature ranges (industrial temperature range: −40 to +85°C, automotive temperature range: −40 to +110°C) is fully compatible with the standard SAB 8051A/8031A with respect to architecture, instruction set, and software portability.

The SAB 8051A/8031A is a stand-alone, high-performance single-chip microcontroller fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

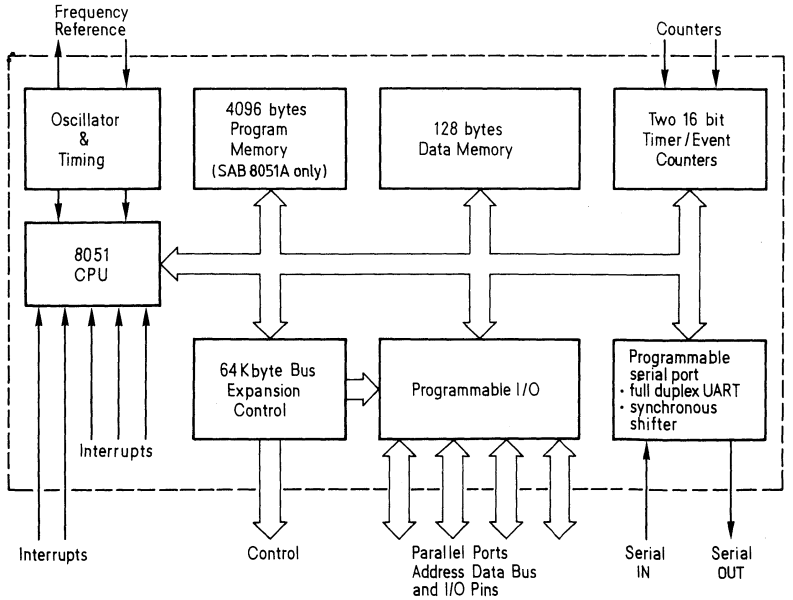
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.0–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification.
RST/VPD	9	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. – $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
XTAL1 XTAL2	19 18		XTAL 1 Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL2. XTAL2 Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification.
$\overline{PSEN}$	29	O	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	O	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{EA}$	31	I	When held at a high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 8051A fetches all instructions from external Program Memory. For the SAB 8031A this pin must be tied low.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#*data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex code	Number of bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	−40 to + 85°C for T40/85 −40 to +110°C for T40/110
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$ $T_A = -40$ to + 85°C for T40/85;
$T_A = -40$ to +110°C for T40/110

Symbol	Parameter	Limit values		Units	Test conditions
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage except RST/VPD and XTAL2	2.0	V_{CC}+0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL2	2.5	V_{CC}+0.5	V	XTAL 1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage ports 1, 2, 3	–	0.45	V	$I_{OL} = 1.6$ mA
V_{OL1}	Output low voltage port 0, ALE, /PSEN	–	0.45	V	$I_{OL} = 3.2$ mA
V_{OH}	Output high voltage ports 1, 2, 3	2.4	–	V	$I_{OH} = -80$ µA
V_{OH1}	Output high voltage port 0, ALE, /PSEN	2.4	–	V	$I_{OH} = -400$ µA
I_{IL}	Logical 0 input current ports 1, 2, 3	–	−500	µA	$V_{IL} = 0.45\,V$
I_{IL2}	Logical 0 input current XTAL2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45\,V$
I_{IH1}	Input high current to RST/VPD for reset	–	500	µA	$V_{IN} = V_{CC} - 1.5\,V$
I_{LI}	Input leakage current to port 0,/EA	–	±10	µA	$0 < V_{IN} < V_{CC}$
I_{CC}	Power supply current	–	150	mA	–
I_{PD}	Power down current	–	15	mA	–
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1$ MHz

AC Characteristics for T40/85

V_{CC} = 5 V ±10%; V_{SS} = 0 V; T_A = −40 to +85°C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2\,t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4\,t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3\,t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3\,t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5\,t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6\,t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6\,t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2\,t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5\,t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2\,t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4\,t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7\,t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 8051A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

AC Characteristics for T40/110

V_{CC} = 5 V ±10%; V_{SS} = 0 V; T_A = −40 to +110°C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	160	–	$2\,t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	70	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	65	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	300	–	$4\,t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	75	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	265	–	$3\,t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	200	–	$3\,t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	80	–	t_{CLCL}-20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	92	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	385	–	$5\,t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

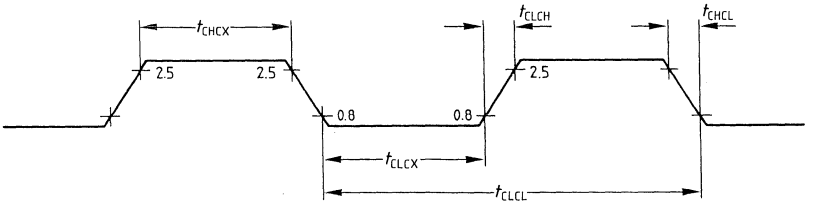
Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	500	–	$6\,t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	500	–	$6\,t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	165	–	$2\,t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	335	–	$5\,t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	130	–	$2\,t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	650	–	$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	735	–	$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	250	350	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	270	–	$4\,t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	60	140	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	50	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	550	–	$7\,t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	50	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 8051A to devices with float times up to 92ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

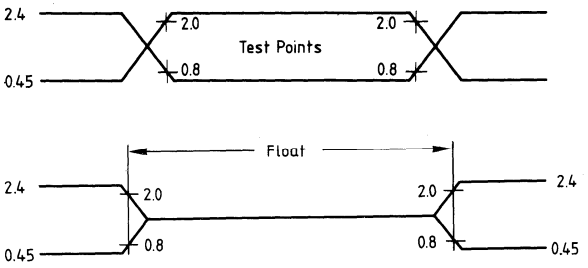
External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz (T40/85) Freq. = 1.2 MHz to 10 MHz (T40/110)		
		min.	max.	
t_{CLCL}	Oscillator period T40/85 T40/110	83.3 100	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



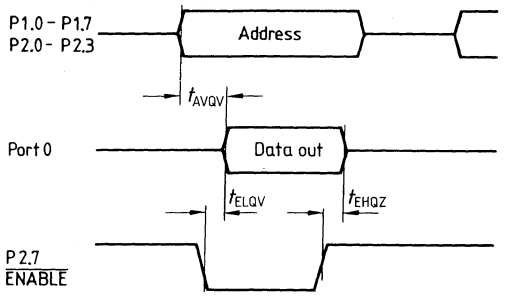
AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{Enable}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{Enable}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

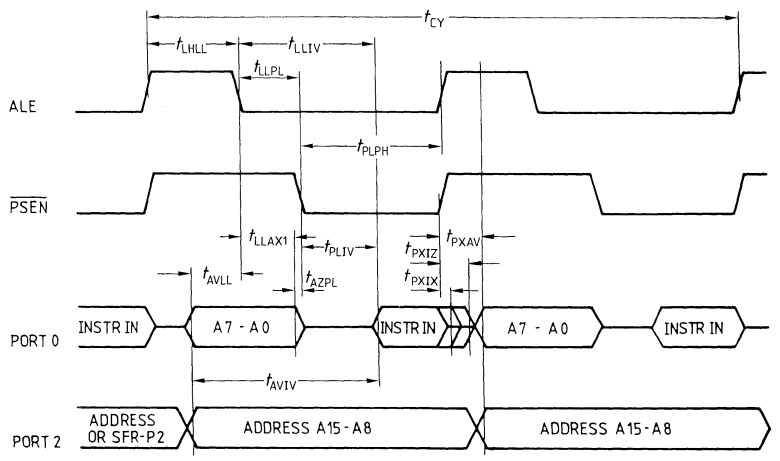


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

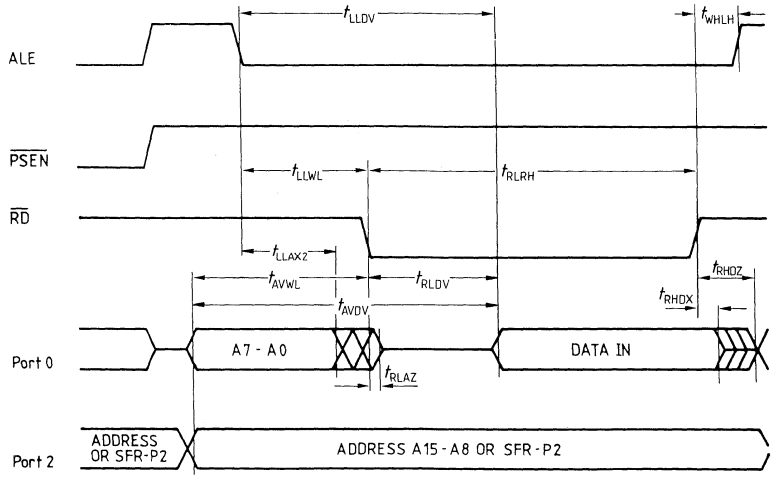
Inputs: P2.4–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
RST/VPD $= V_{IH1}$

Waveforms

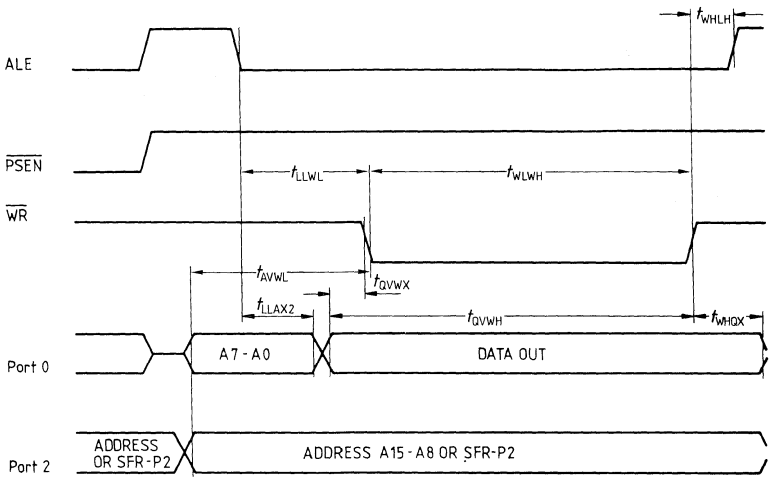
Program Memory Read Cycle



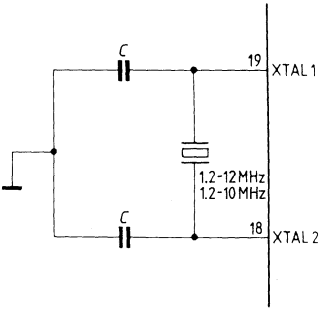
Data Memory Read Cycle



Data Memory Write Cycle

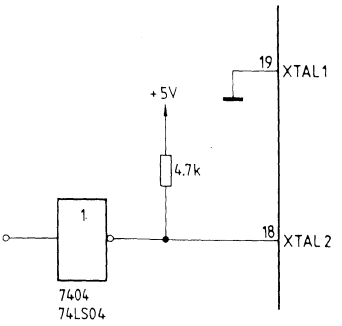


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

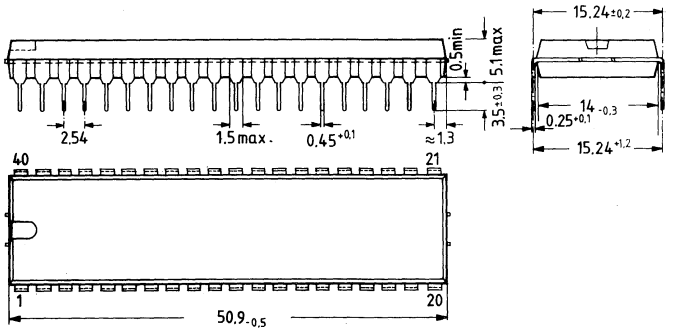
Crystal Oscillator Mode



Driving from External Source

Package Outlines

Plastic Package, P-DIP 40, 20 B 40 DIN 41870 T 10



Dimensions in mm

Ordering Information

Type	Description	Ordering code
	8-Bit Single-Chip-Microcomputer	
SAB 8051A-12-P-T40/85	with mask-programmable ROM (Plastic)	Q 67120-C233
SAB 8051A-10-P-T40/110	with mask-programmable ROM (Plastic)	Q 67120-C231
SAB 8031A-12-P-T40/85	for external Memory (Plastic)	Q 67120-C230
SAB 8031A-10-P-T40/110	for external Memory (Plastic)	Q 67120-C232

Advance Information

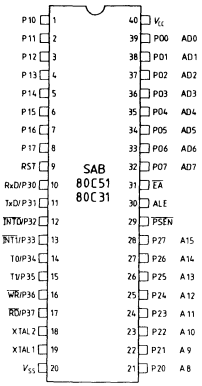
SAB 80C51/80C31 Ext. Temp. 8-Bit CMOS Microcontroller

SAB 80C51-P(N)-T40/85 CMOS microcontroller with factory-mask programmable ROM, P-DIP 40 (PLCC 44)
SAB 80C31-P(N)-T40/85 CMOS microcontroller for external ROM, P-DIP 40 (PLCC 44)

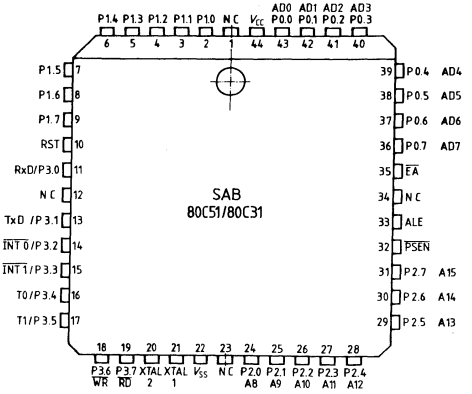
- Extended operating temperature range: −40 to +85°C
- 4K × 8 ROM (SAB 80C51 only)
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable up to 128 Kbytes
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- 5 interrupt vectors, two priority levels
- Idle and power-down operation
- P-DIP 40 and PLCC 44 package

Pin Configuration

P-DIP 40



PLCC 44



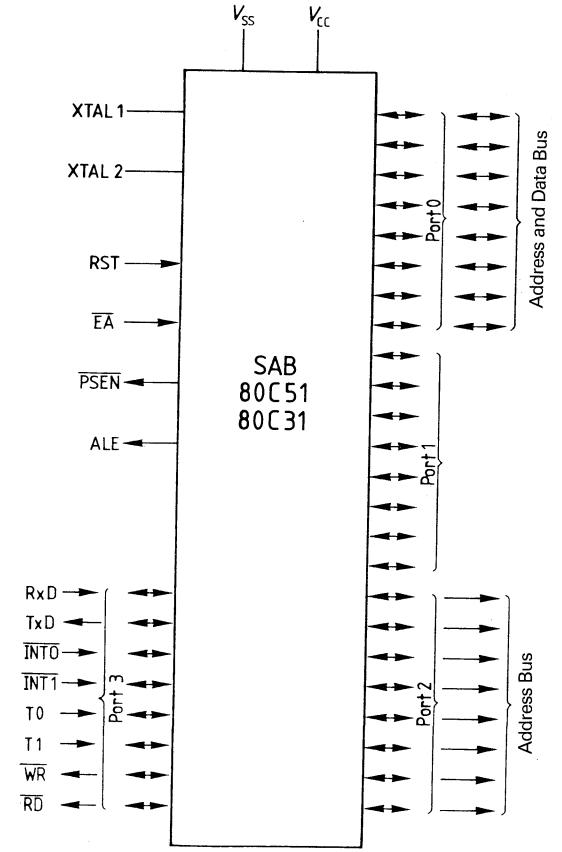
The SAB 80C51/80C31 is a standalone, high-performance CMOS single-chip microcontroller, designed in Siemens ACMOS technology. It is functionally compatible with the SAB 8051A/8031A devices in MYMOS technology. The version with extended operating temperature range is fully compatible with the standard device SAB 80C51/80C31.

The low-power properties of ACMOS technology allow applications where power consumption and dissipation are critical. In addition, the SAB 80C51/80C31 has two software-selectable modes of reduced activity for further power reduction – idle and power-down.

The SAB 80C51 contains a non-volatile 4K × 8 read-only program memory, a volatile 128 × 8 read/write data memory, 32 I/O lines, two 16-bit timer/counters, a five-vector, two-priority-level interrupt structure, a serial I/O port, an on-chip oscillator, and clock circuits. The SAB 80C31 is identical to the SAB 80C51, except that it lacks the program memory on the chip.

The SAB 80C51/80C31 is supplied in a 40-pin plastic DIP package or in a 44-pin plastic leaded chip carrier (PLCC 44) package.

Logic Symbol



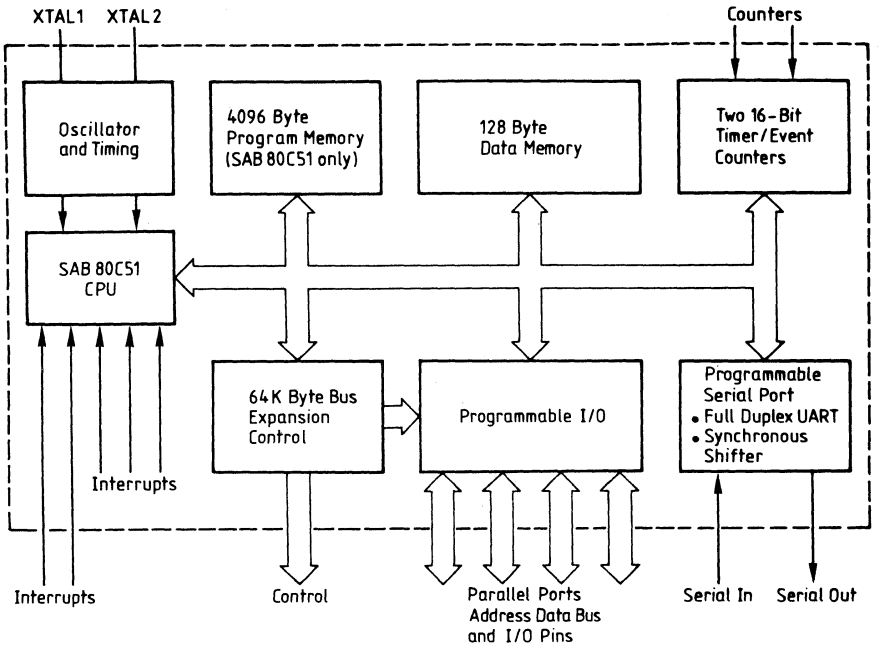
Pin Definitions and Functions

Symbol	Pin P-DIP40	Pin PLCC44	Input (I) Output (O)	Functions
P1.0–P1.7	1–8	2–9	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 1 also receives the low-order address bytes during program verification.
RST	9	10	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – $\overline{RxD}$/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – $\overline{TxD}$/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20		XTAL 1 Input to the inverting oscillator amplifier and input to the internal clock generator circuits. XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL 2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-DIP40	Pin PLCC44	Input (I) Output (O)	Functions
P2.0–P2.7	21–28	24–31	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	29	32	O	$\overline{\text{PROGRAM STORE ENABLE}}$ This output issues a control signal that enables the external program memory to access the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	ADDRESS LATCH ENABLE Provides signal used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	31	35	I	$\overline{\text{EXTERNAL ACCESS}}$ When held at a high level, the SAB 80C51 executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 80C51 fetches all instructions from the external program memory. For the SAB 80C31 this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C51. External pullup resistors are required during program verification.
V_{CC}	40	44		Supply voltage during normal, idle, and power-down operations.
V_{SS}	20	22		Circuit ground potential.
N.C.	–	1, 12, 23, 34	–	No connection

Block Diagram



Functional Description

The SAB 80C51/80C31 is functionally compatible with the SAB 8051A/8031A products that are designed in Siemens MYMOS technology.

In addition, instead of the RAM backup power supply of the SAB 8051A/8031A, the SAB 80C51/80C31 offers two additional power control modes, the idle mode and the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

- Idle mode
  In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction that invokes the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The contents of the CPU, the on-chip RAM, and all the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor in the same way as a power-on reset.
- Power-down mode
  In the power-down mode the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. Only the contents of the on-chip RAM is preserved. A hardware reset is the only way to terminate power-down.

During power-down and idle mode the external pins will have the following status (see table 1):

Table 1
Status of the External Pins during Idle and Power-Down Modes

Mode	Program Memory	ALE	PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data	Data	Data/ Alternate Outputs
Idle	External	1	1	Float	Data	Address	Data/ Alternate Outputs
Power-Down	Internal	0	0	Data	Data	Data	Data/Last Output of Alternate Function
Power-Down	External	0	0	Float	Data	Data	Data/Last Output of Alternate Function

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn — Working register R0–R7
direct — 128 internal RAM locations, any I/O port, control or status register
@Ri — Indirect internal or external RAM location addressed by register R0 or R1
#data — 8-bit constant included in instruction
#data 16 — 16-bit constant included as bytes 2 and 3 of instruction
bit — 128 software flags, any I/O pin, control or status bit
A — Accumulator

Notes on program addressing modes:

addr 16 — Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 — Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A, ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	−40 to +85°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 V to V_{CC} +0.5 V
Voltage on V_{CC} to V_{SS}	−0.5 to 6.5 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 20\%$; $V_{SS} = 0\,V$; $T_A = -40$ to $+85°C$

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
V_{IL}	Input low voltage (except EA)	−0.5	$0.2V_{CC}-0.1$	V	–
V_{IL1}	Input low voltage (EA)	−0.5	$0.2V_{CC}-0.3$	V	–
V_{IH}	Input high voltage (except XTAL1, RST)	$0.2V_{CC}+0.9$	$V_{CC}+0.5$	V	–
V_{IH1}	Input high voltage (XTAL1, RST)	$0.7V_{CC}$	$V_{CC}+0.5$	V	–
V_{OL}	Output low voltage (ports 1, 2, 3)	–	0.45	V	$I_{OL} = 1.6$ mA [1]
V_{OL1}	Output low voltage (port 0, ALE, PSEN)	–	0.45	V	$I_{OL} = 3.2$ mA [1]
V_{OH}	Output high voltage (ports 1, 2, 3)	2.4	–	V	$I_{OH} = -60\,\mu A$ $V_{CC} = 5V \pm 10\%$
		$0.75V_{CC}$	–	V	$I_{OH} = -25\,\mu A$
		$0.9V_{CC}$	–	V	$I_{OH} = -10\,\mu A$
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, PSEN)	2.4	–	V	$I_{OH} = -400\,\mu A$ $V_{CC} = 5V \pm 10\%$
		$0.75V_{CC}$	–	V	$I_{OH} = -150\,\mu A$
		$0.9V_{CC}$	–	V	$I_{OH} = -40\,\mu A$ [2]
I_{IL}	Logical 0 input current (ports 1, 2, 3)	–	−50	µA	$V_{IN} = 0.45V$
I_{TL}	Logical 1-to-0 transition current (ports 1, 2, 3)	–	−650	µA	$V_{IN} = 2V$
I_{LI}	Input leakage current (port 0, EA)	–	±10	µA	$0.45 < V_{IN} < V_{CC}$
R_{RST}	Reset pulldown resistor	50	150	kΩ	–
C_{IO}	Pin capacitance	–	10	pF	$f_c = 1$ MHz, $T_A = 25°C$
I_{PD}	Power down current	–	50	µA	$V_{CC} = 2$ to 6V [3]

For notes refer to next page.

DC Characteristics (cont'd)

Maximum I_{CC} (mA)

		Active Mode [4]			Idle Mode [5]		
Freq.	V_{CC}	4 V	5 V	6 V	4 V	5 V	6 V
0.5 MHz		TBD	TBD	TBD	TBD	TBD	TBD
3.5 MHz		TBD	TBD	TBD	TBD	TBD	TBD
8.0 MHz		TBD	TBD	TBD	TBD	TBD	TBD
12 MHz		TBD	28	TBD	TBD	12	TBD

Note 1: Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading >100pF), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

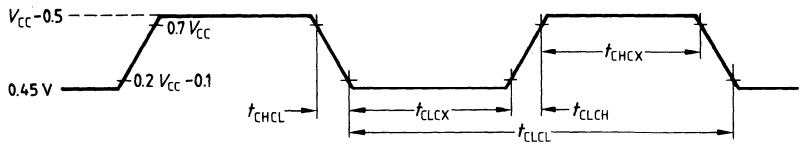
Note 2: Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stable.

Note 3: Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = V_{CC}; XTAL1 = V_{SS}; XTAL2 = N.C.; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

Note 4: I_{CC} (active mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = Port 0 = V_{CC}; $\overline{RESET}$ = V_{CC}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

Note 5: I_{CC} (idle mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = V_{CC}; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode
$t_{CLCH} = t_{CHCL}$ = 5 ns



AC Characteristics

$T_A = -40$ to $+85°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	28	–	t_{CLCL}-55	–	ns
t_{LLAX}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	234	–	$4t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	43	–	t_{CLCL}-40	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	205	–	$3t_{CLCL}$-45	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	145	–	$3t_{CLCL}$-105	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	Input instruction float after $\overline{PSEN}$	–	59	–	t_{CLCL}-25	ns
t_{AVIV}	Address to valid instruction in	–	312	–	$5t_{CLCL}$-105	ns
t_{PLAZ}	$\overline{PSEN}$ to address float	–	10	–	10	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{AVWL}	Address valid to $\overline{WR}$	203	–	$4t_{CLCL}$-130	–	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	23	–	t_{CLCL}-60	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive

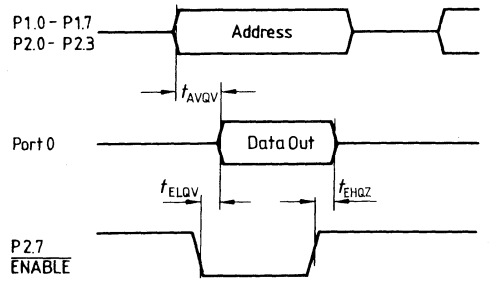
Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 0.5 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	2000	ns
t_{CHCX}	High time	20	–	ns
t_{CLCX}	Low time	20	–	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns
$1/t_{CLCL}$	Oscillator frequency	0.5	12	MHz

ROM Verification Characteristics for SAB 80C51

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

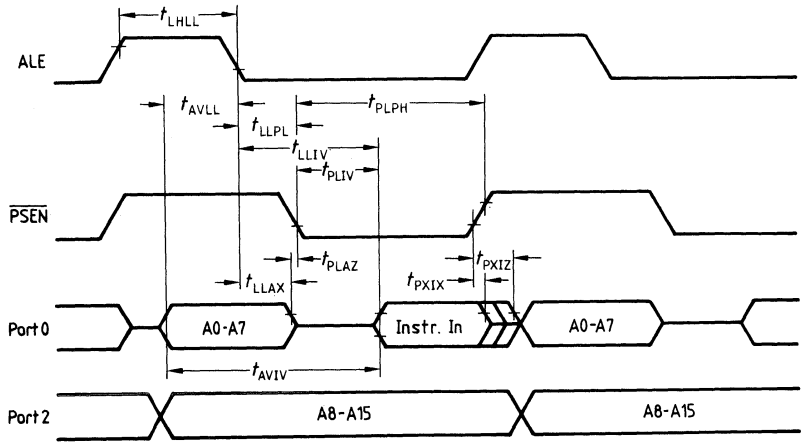


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

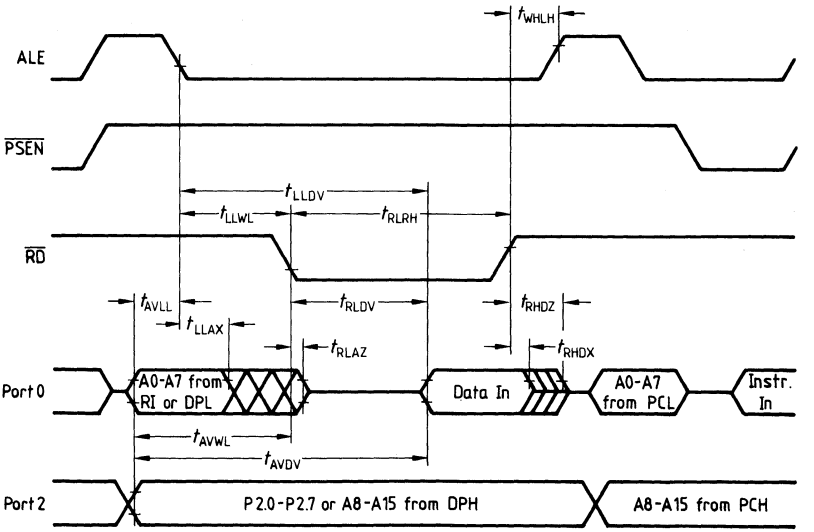
Inputs: P2.4–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
RST $= V_{IH1}$

Waveforms

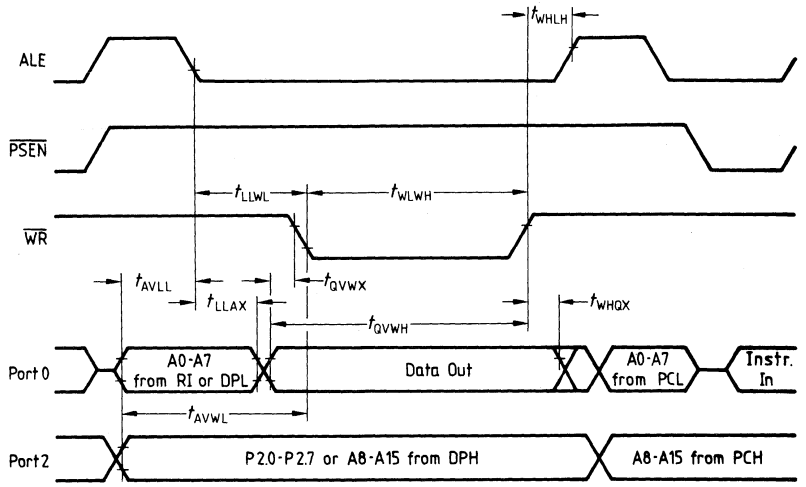
Program Memory Read Cycle



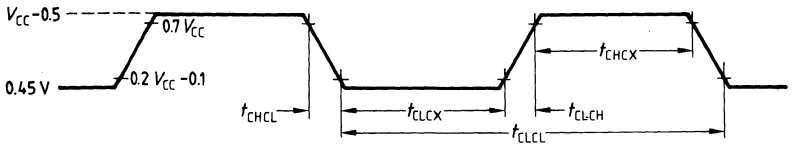
Data Memory Read Cycle



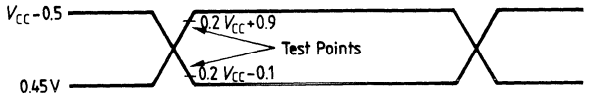
Data Memory Write Cycle



External Clock Cycle

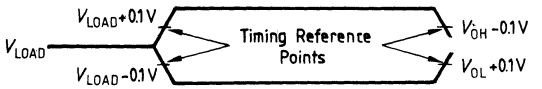


AC Testing: Input, Output Waveforms



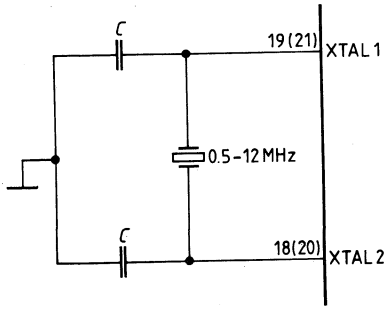
AC Inputs during testing are driven at $V_{CC}-0.5V$ for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at $V_{IH\,min}$ for a logic '1' and $V_{IL\,max}$ for a logic '0'.

AC Testing: Float Waveforms



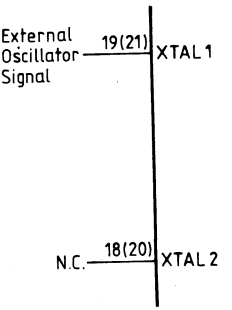
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

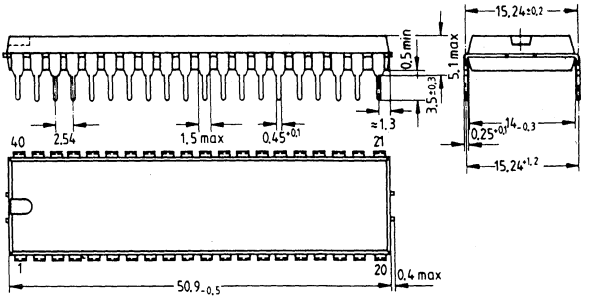


Driving from External Source

Pin numbers in (...) are for PLCC 44 package

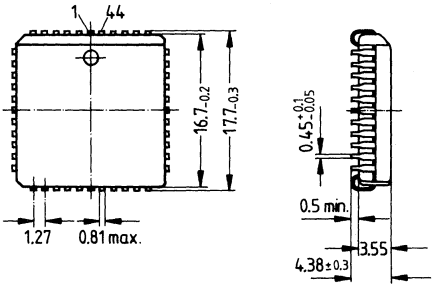
Package Outlines

Plastic Package, P-DIP, 40 pins



Dimensions in mm

Plastic Package, PLCC, 44 pins



Dimensions in mm

Ordering Information

Type	Ordering code	Function
		8-bit CMOS microcontroller
SAB 80C51-P-T40/85	Q 67120-C389	with mask-programmable ROM (P-DIP 40)
SAB 80C31-P-T40/85	Q 67120-C390	for external memory (P-DIP 40)
SAB 80C51-N-T40/85	Q67120-C393	with mask-programmable ROM (PLCC 44)
SAB 80C31-N-T40/85	Q67120-C392	for external memory (PLCC 44)

Preliminary

SAB 8052A/8032A Ext.Temp. 8-Bit Single-Chip Microcontroller

Extended Temperature Range: −40° to + 85°C
−40° to +100°C

SAB 8052A-T40/85
SAB 8052A-T40/100 with mask-programmable ROM

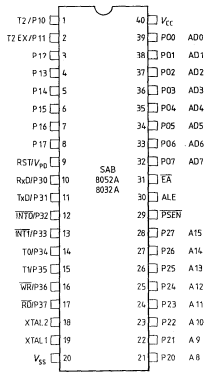
- 8K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes

SAB 8032A-T40/85
SAB 8032A-T40/100 for external ROM

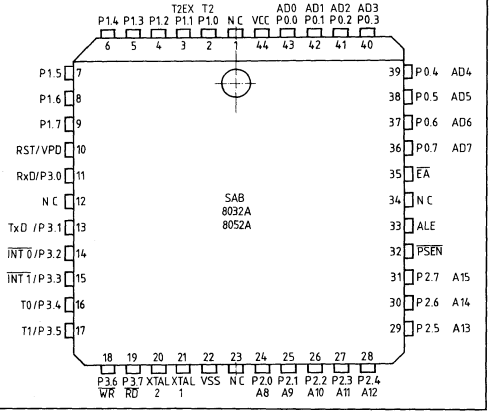
- Boolean processor
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- P-DIP40 and PLCC44 package
- Full backward compatibility with SAB 8051/8031

Pin Configuration

P-DIP40



PLCC44

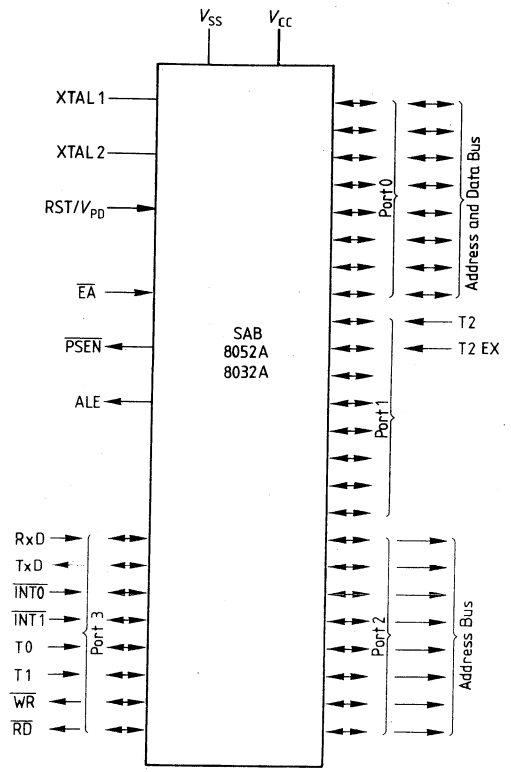


The SAB 8052A/8032A for the two extended temperature ranges −40 to +85°C and −40 to +100°C is fully compatible with the standard SAB 8052A/8032A with respect to architecture, instruction set, and software portability.
The SAB 8052A/8032A is a standalone, high-performance single-chip microcontroller fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology. Both extended temperature versions are available in a 40-pin plastic DIP (P-DIP 40) package: The SAB 8052A-T40/85 is also supplied in a 44-pin plastic leaded chip carrier (PLCC44) package.

The SAB 8052A contains a non-volatile 8 K × 8 read-only program memory; a volatile 256 × 8 read/write data memory; 32 I/O lines; three 16-bit timer/counters; a six-source, two-priority level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical with the SAB 8052A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8052A can be expanded using standard TTL-compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Logic Symbol



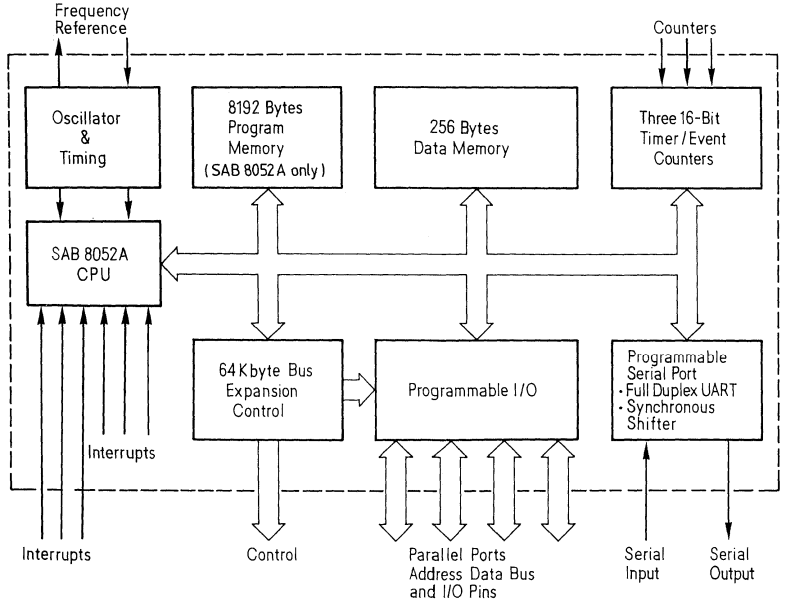
Pin Definitions and Functions

Symbol	Pin DIP40	Pin PLCC44	Input (I) Output (O)	Function
P1.0–P1.7	1–8	2–9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – R×D/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – T×D/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19, 18	21, 20		XTAL 1 input to the oscillator's high-gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	24–31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin DIP40	Pin PLCC44	Input (I) Output (O)	Function
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied low.
P0.0–P0.7	39–32	43–36	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+5V power supply during operation and program verification.
V_{SS}	20	22	–	Circuit ground potential
NC	–	1, 12, 23, 24	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#*data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	−40 to + 85°C for T40/85 −40 to +100°C for T40/100
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $T_A = -40$ to + 85°C for T40/85;
$T_A = -40$ to +100°C for T40/100;

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power-down voltage to RST/V_{PD}	4.5	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	$I_{OL} = 1.6$ mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	$I_{OL} = 3.2$ mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	$I_{OH} = -80$ µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	$I_{OH} = -400$ µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	−500	µA	$V_{IL} = 0.45$ V
I_{IL2}	Logical 0 input current XTAL 2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45$ V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	$V_{IN} = V_{CC} - 1.5$ V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	$0V < V_{IN} < V_{CC}$
I_{CC}	Power supply current	–	175	mA	All outputs disconnected
I_{PD}	Power-down current	–	15	mA	$V_{CC} = 0\,V$
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1$ MHz

AC Characteristics for T40/85

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $T_A = -40°$ to $+85°C$
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} [1]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} [1]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

[1]) Interfacing the SAB 8052A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for T40/100

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = −40° to + 100°C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	160	–	$2t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	70	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	65	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	300	–	$4t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	75	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	265	–	$3t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instructrion in	–	200	–	$3t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} [1]	Input instruction float after $\overline{PSEN}$	–	80	–	t_{CLCL}-20	ns
t_{PXAV} [1]	Address valid after $\overline{PSEN}$	92	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	385	–	$5t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

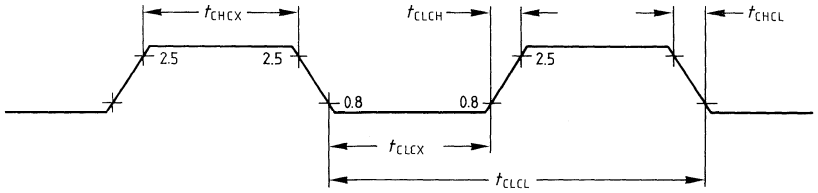
Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	500	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	500	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	165	–	$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	335	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	130	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	650	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	735	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	250	350	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	270	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	60	140	t_{CLCL}-40	t_{CLCL}+40	ns
t_{DVWX}	Data valid to $\overline{WR}$ transition	50	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	550	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	50	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

[1]) Interfacing the SAB 8052A to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

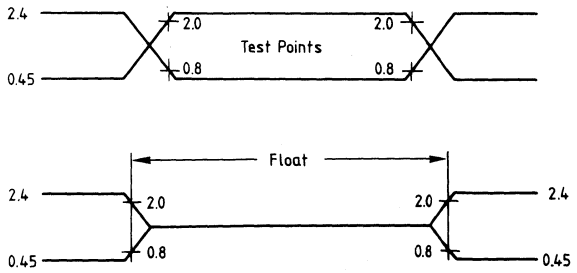
External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz (T40/85) Freq. = 1.2 MHz to 10 MHz (T40/100)		
		min.	max.	
t_{CLCL}	Oscillator period T40/85 T40/100	83.3 100	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{TCHCL}	Fall time	–	20	ns

External Clock Cycle



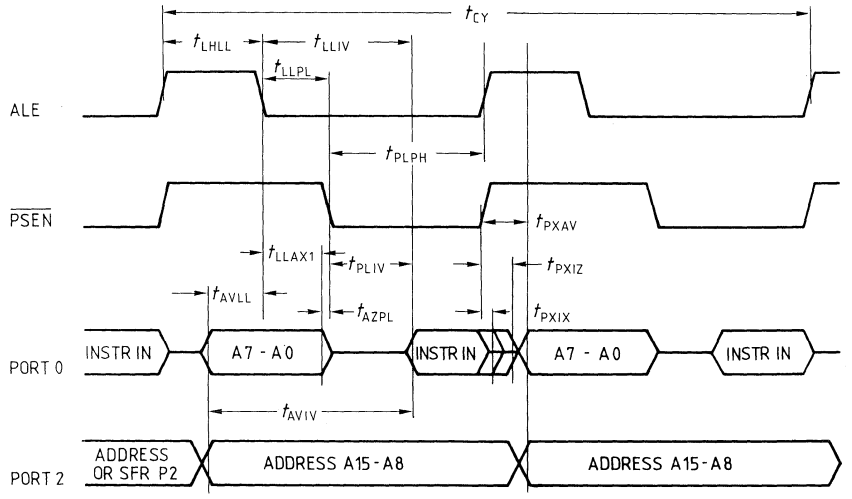
AC Testing Input, Output, Float Waveforms



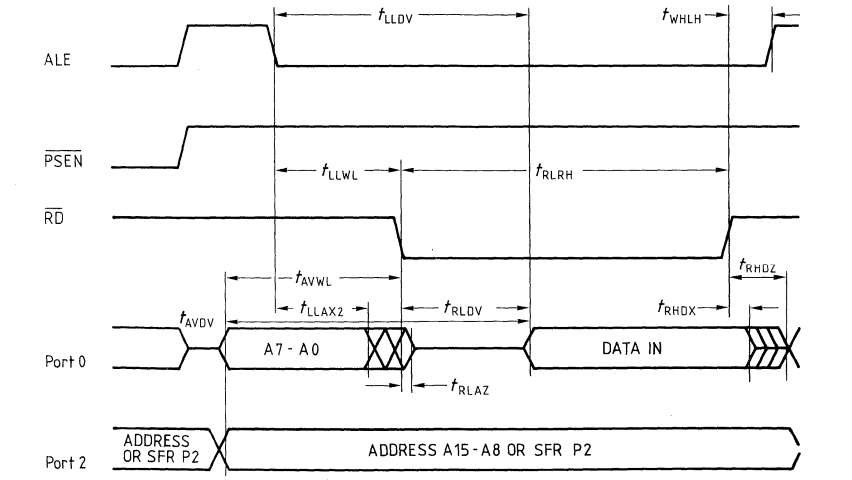
AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

Waveforms

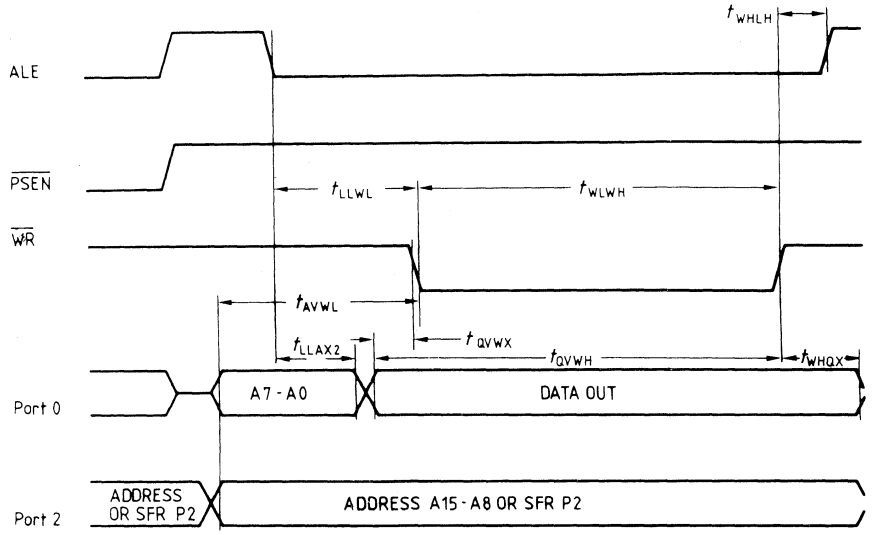
Program Memory Read Cycle



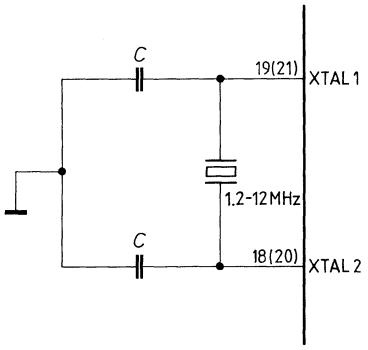
Data Memory Read Cycle



Data Memory Write Cycle

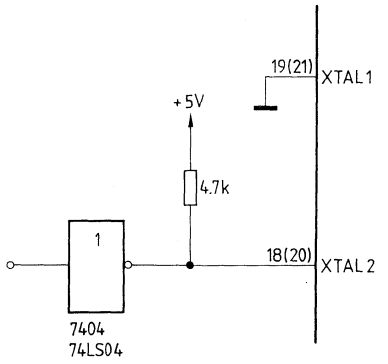


Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode



Driving from External Source

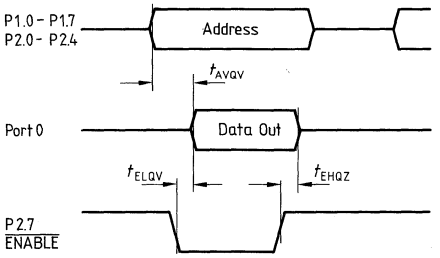
Pin numbers in (...) are specified for PLCC44 package.

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



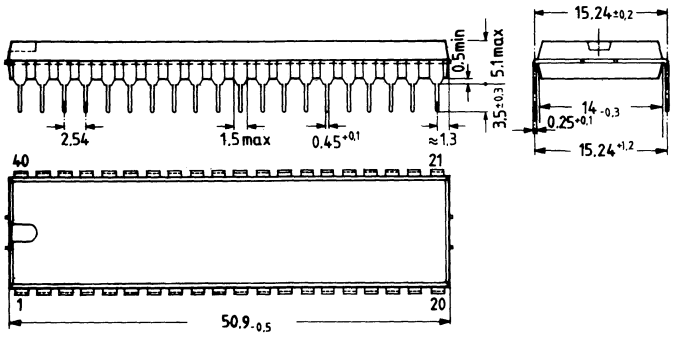
Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

Inputs: P2.5–P2.6, $\overline{\text{PSEN}} = V_{SS}$
ALE, $\overline{\text{EA}} = V_{IH}$
RST/$V_{PD} = V_{IH1}$

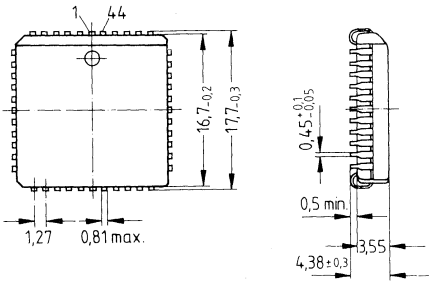
Package Outlines

Plastic Package, P-DIP, 40 Pins



Dimensions in mm

Plastic Package, PLCC, 44 Pins



Dimensions in mm

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcontroller
SAB 8052A-P-T40/85	Q 67120-C247	with mask-programmable ROM (P-DIP40)
SAB 8052A-P-T40/100	Q 67120-C248	with mask-programmable ROM (P-DIP40)
SAB 8032A-P-T40/85	Q 67120-C235	for external memory (P-DIP40)
SAB 8032A-P-T40/100	Q 67120-C239	for external memory (P-DIP40)
SAB 8052A-N-T40/85	Q 67120-C368	with mask programmable ROM (PLCC44)
SAB 8032A-N-T40/85	Q 67120-C367	for external memory (PLCC44)

Preliminary

SAB 80515/80535 Ext.Temp. 8-Bit Single-Chip Microcontroller

Extended Temperature Ranges:

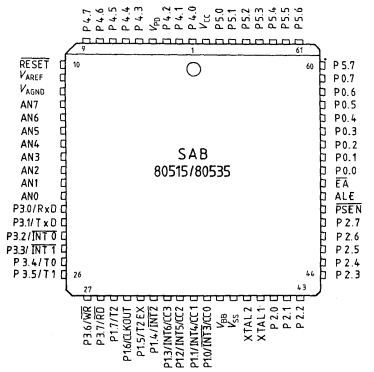
T40/85	**−40°C to + 85°C**	**12 MHz operation**
T40/110	**−40°C to +110°C**	**10 MHz operation**

SAB 80515-N-T40/85
SAB 80515-N-T40/110 — **Microcontroller with factory mask-programmable ROM**

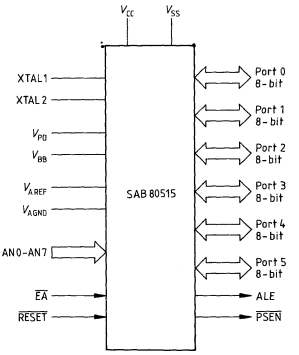
SAB 80535-N-T40/85
SAB 80535-N-T40/110 — **Microcontroller for external ROM**

- Version of the SAB 80515/80535 for two extended temperature ranges
- 8K × 8 ROM (SAB 80515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with eight multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Backwardly compatible with SAB 8051
- 68-pin plastic leaded chip carrier package (PLCC 68)

Pin Configuration



Logic Symbol



The SAB 80515/80535 Ext. Temp. is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. The SAB 80515/80535 Ext. Temp. is available for the industrial temperature range (−40 to +85°C) and the automotive temperature range (−40 to +110°C). It is fully compatible with the standard SAB 80515/80535 with respect to architecture, instruction set and software portability. The SAB 80515/80535 Ext. Temp. is a stand-alone, high-performance single-chip microcontroller designed in +5V N-channel, silicon-gate Siemens MYMOS technology. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 Ext. Temp. incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 Ext. Temp. is supplied in a 68-pin plastic leaded chip carrier package (PLCC 68).

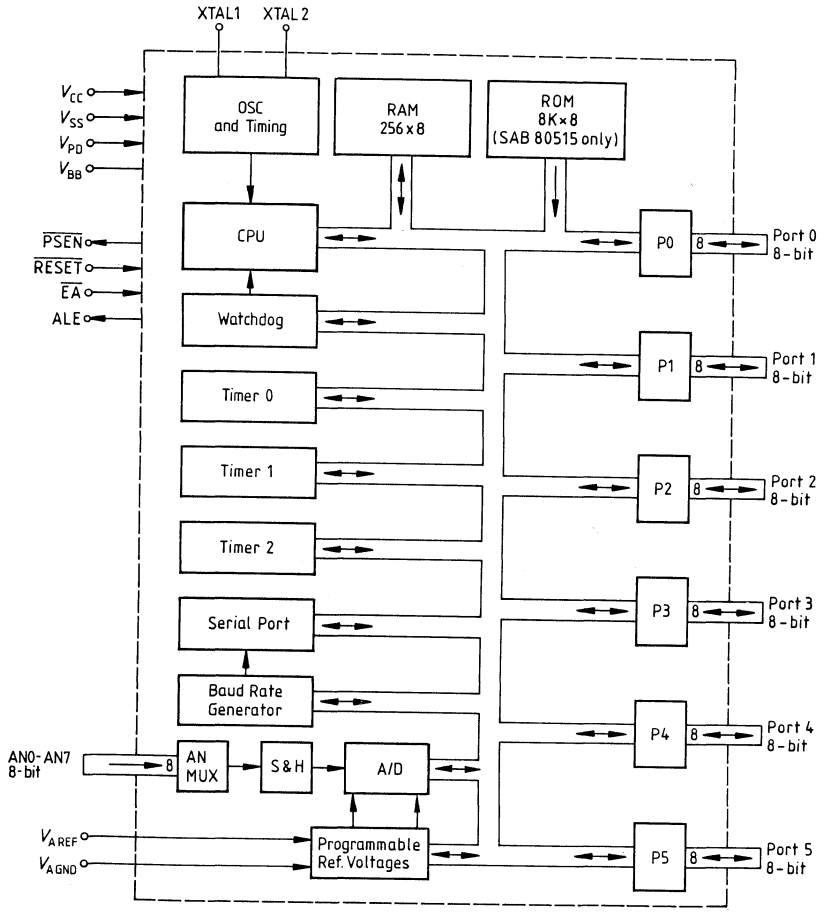
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4		Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0 (cont'd)			– $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39		XTAL2 is the output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40		XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+5V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via this interface substitutes the SAB 80515's internal ROM.

The SAB 80535 is identical to the SAB 80515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80515" is used to refer to both the SAB 80515 and SAB 80535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described below:
(Figure 2 illustrates the memory address spaces of the SAB 80515).

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external programm memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

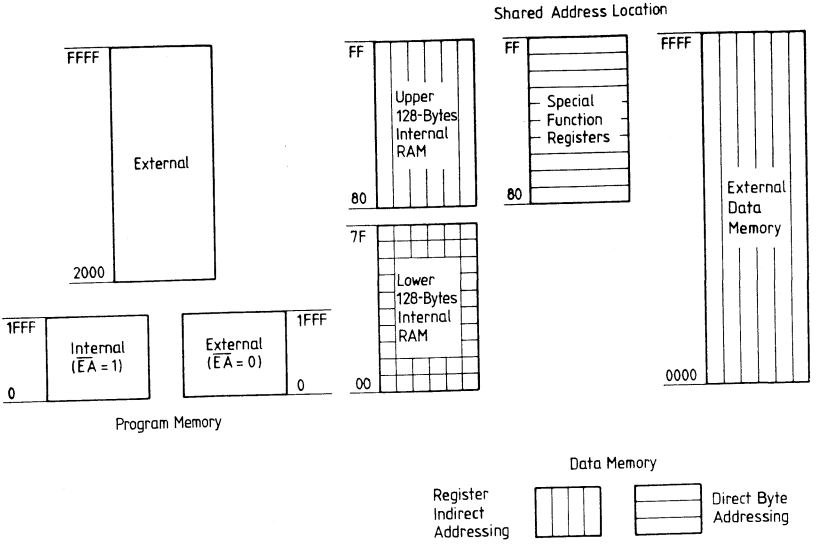
The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D-converter control register	0D8H
ADDAT	A/D-converter data register	0D9H
DAPR	D/A-converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input. Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0–AN7 is used for analog input signals to the A/D converter.

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 3 shows a block diagram of the timer/counter 2.

– Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

– Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

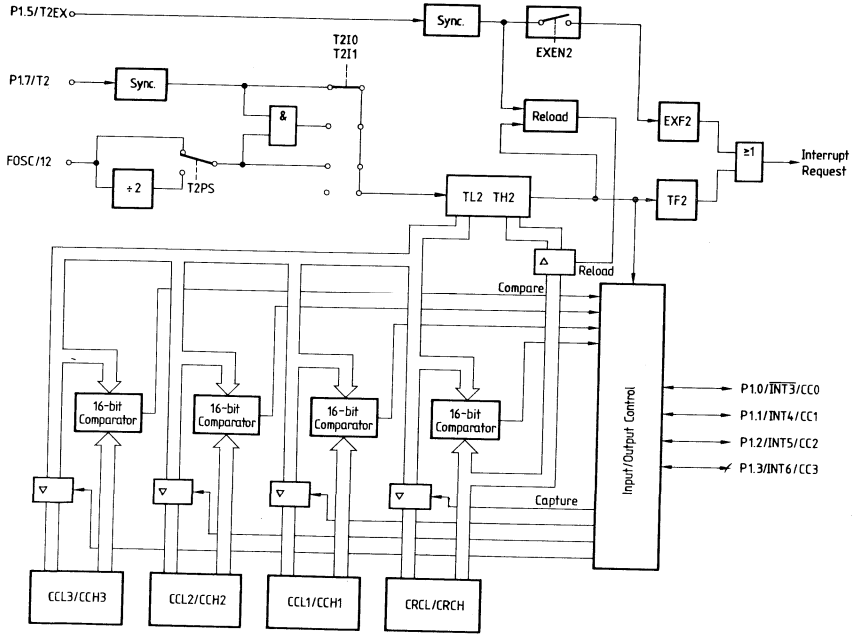
– Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

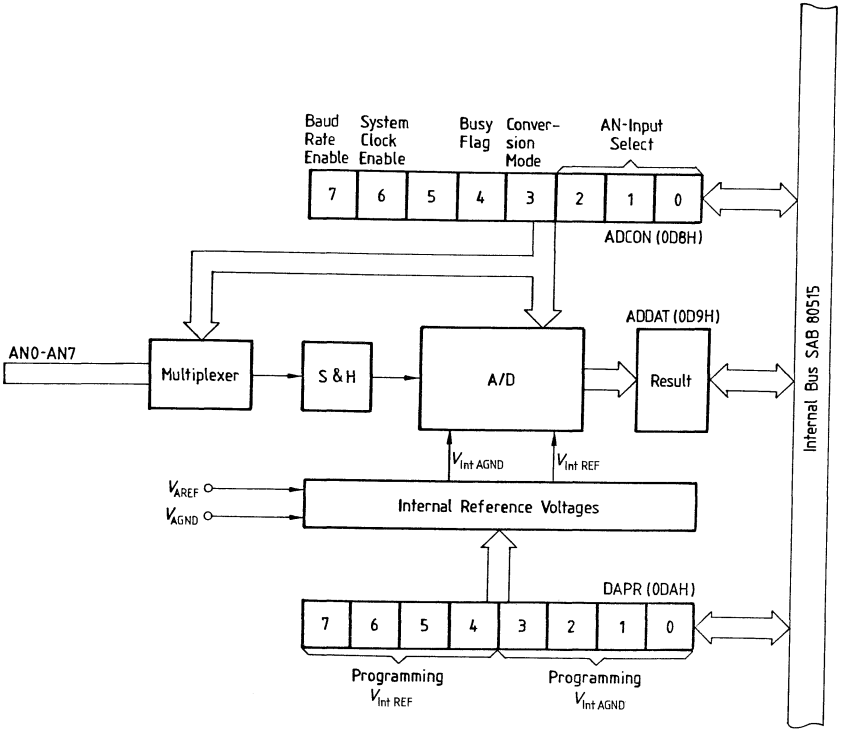
A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 14 machine cycles (14 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/ disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

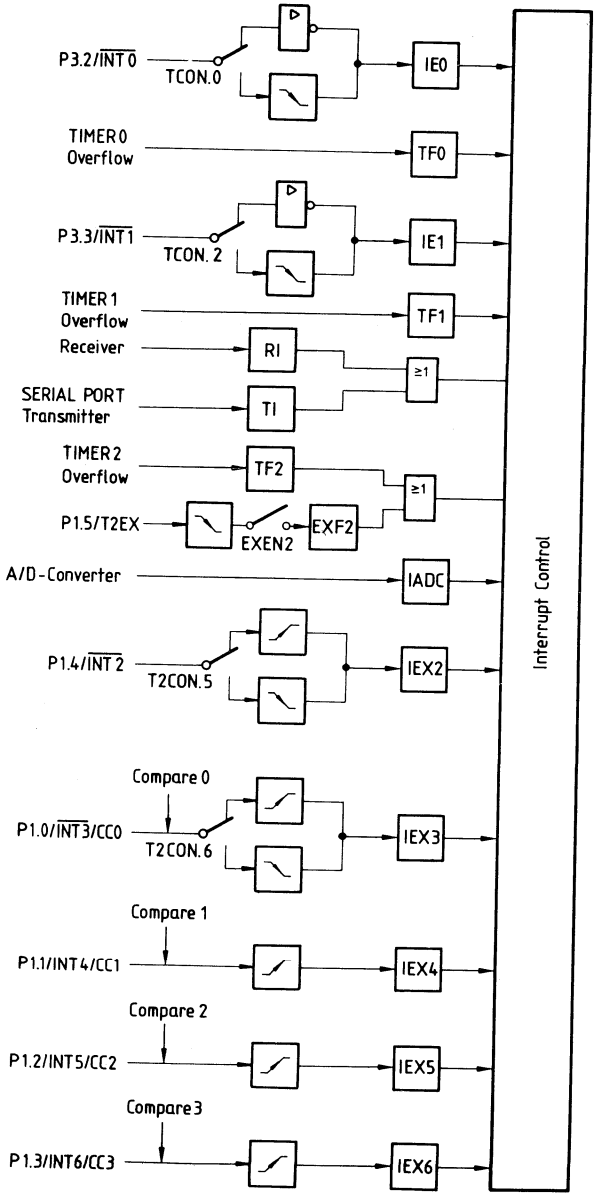
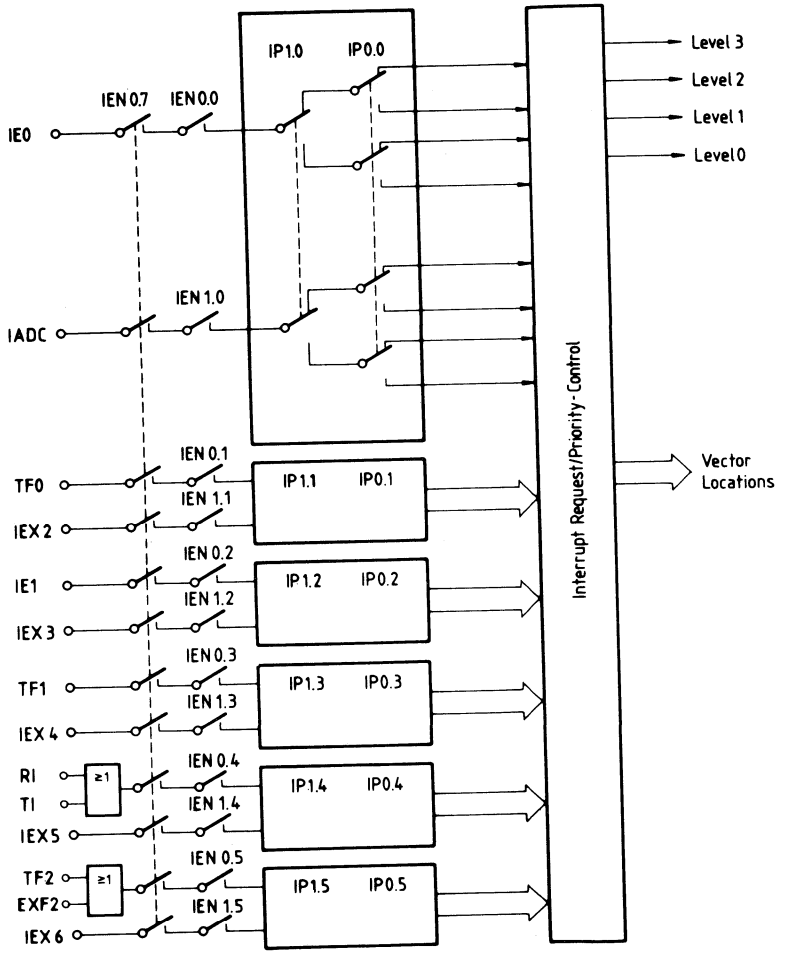


Figure 6
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN 0.6 and IEN 1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to accumulator	1	1
ADD	A, direct	Add direct byte to accumulator	2	1
ADD	A, @Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	−40 to + 85°C for SAB 80515/80535-T40/85 −40 to +110°C for SAB 80515/80535-T40/110
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $T_A = -40$ to $+85°C$; for SAB 80515/80535-T40/85
$T_A = -40$ to $+110°C$ for SAB 80515/80535-T40/110

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{RESET}$ and XTAL2)	2.0	$V_{CC}+0.5$	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	$V_{CC}+0.5$	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{RESET}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	$I_{OL} = 1.6\,mA$
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$	–	0.45	V	$I_{OL} = 3.2\,mA$
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	$I_{OH} = -80\,\mu A$
V_{OH1}	Output high voltage, port 0, ALE, $\overline{PSEN}$	2.4	–	V	$I_{OH} = -400\,\mu A$
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	−800	µA	$V_{IL} = 0.45\,V$
I_{IL2}	Logic 0 input current, XTAL2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45\,V$
I_{IL3}	Input low current to $\overline{RESET}$ for reset	–	−500	µA	$V_{IL} = 0.45\,V$
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	±10	µA	$0\,V < V_{IN} < V_{CC}$
I_{CC}	Power supply current SAB 80515/80535-T40/85 SAB 80515/80535-T40/110	 – –	 230 230	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	$V_{CC} = 0\,V$
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1\,MHz$

A/D Converter Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V; V_{AREF} = V_{CC} ±5%; V_{AGND} = V_{SS} ±0.2V; $V_{IntAREF} - V_{IntAGND} \geq 1$V;
T_A = −40 to +85°C for SAB 80515/80535-T40/85
T_A = −40 to +110°C for SAB 80515/80535-T40/110

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND}− 0.2	–	V_{AREF}+ 0.2	V	–
C_I	Analog input capacitance	–	25	–	pF	1)
t_L	Load time	–	–	2 t_{CY}	–	–
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	–	–
t_C	Conversion time (including sample time)	–	–	15 t_{CY}	–	–
DNLE	Differential non-linearity	–	±1/2	±1	LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS}
INLE	Integral non-linearity	–	±1/2	±1	LSB	
	Offset error		±1/2	±1	LSB	
	Gain error	–	±1/2	±1	LSB	
TUE	Total unadjusted error	–	–	±2	LSB	2)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)
$V_{Int\ REF\ ERR}$	Internal reference error	–	±5	±15	mV	2)

Note 1): The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) during load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

Note 2): The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics for T40/85

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$
$T_A = -40$ to $+85°C$ for SAB 80515/80535-T40/85
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	12 t_{CLCL}	–	ns
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL}-40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	4 t_{CLCL}-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	3 t_{CLCL}-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	3 t_{CLCL}-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	5 t_{CLCL}-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	6 t_{CLCL}-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	6 t_{CLCL}-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL}-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	5 t_{CLCL}-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	2 t_{CLCL}-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	8 t_{CLCL}-150	ns
t_{AVDV}	Address to valid data in	–	585	–	9 t_{CLCL}-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3 t_{CLCL}-50	3 t_{CLCL}+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4 t_{CLCL}-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	7 t_{CLCL}-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 80515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for T40/110

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$
$T_A = -40$ to $+110°C$ for SAB 80515/80535-T40/110
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	160	–	$2\,t_{CLCL}$-40	–	ns
t_{AVLL}	Address setup to ALE	70	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	65	–	t_{CLCL}-35	–	ns
t_{LLIV}	ALE to valid instruction in	–	300	–	$4\,t_{CLCL}$-100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	75	–	t_{CLCL}-25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	265	–	$3\,t_{CLCL}$-35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	200	–	$3\,t_{CLCL}$-100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	80	–	t_{CLCL}-20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	92	–	t_{CLCL}-8	–	ns
t_{AVIV}	Address to valid instruction in	–	385	–	$5\,t_{CLCL}$-115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

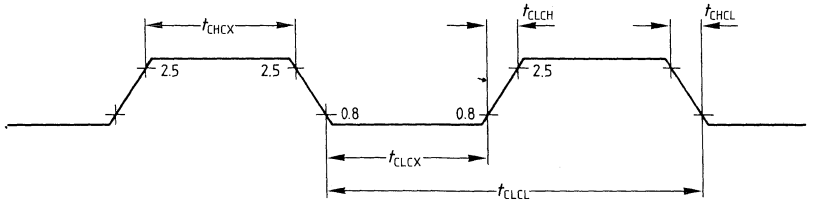
Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	500	–	$6\,t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	500	–	$6\,t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	165	–	$2\,t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	335	–	$5\,t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	130	–	$2\,t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	650	–	$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	735	–	$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	250	350	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	270	–	$4\,t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	60	140	t_{CLCL}-40	t_{CLCL}+40	ns
t_{DVWX}	Data valid to $\overline{WR}$ transition	50	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	550	–	$7\,t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	50	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 80515 to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

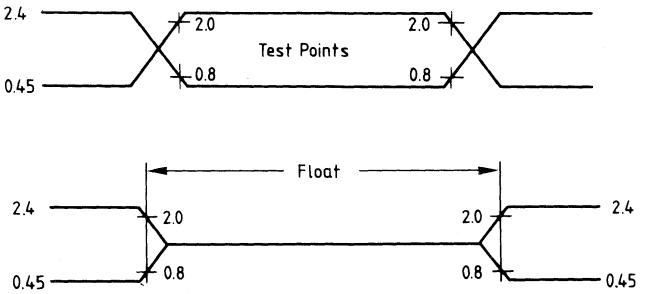
External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz (T40/85) Freq. = 1.2 MHz to 10 MHz (T40/110)		
		min.	max.	
t_{CLCL}	Oscillator period T40/85 T40/110	83.3 100	833.3 833.3	ns ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCX}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

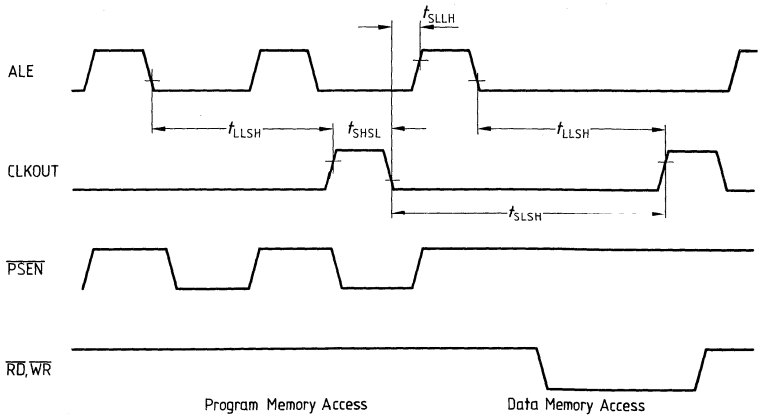
System Clock Timing for T40/85

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LLSH}	ALE to CLKOUT	543	–	7 t_{CLCL}-40	–	ns
t_{SHSL}	CLKOUT high time	127	–	2 t_{CLCL}-40	–	ns
t_{SLSH}	CLKOUT low time	793	–	10 t_{CLCL}-40	–	ns
t_{SLLH}	CLKOUT low to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns

System Clock Timing for T40/110

Symbol	Parameter	Limit values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{LLSH}	ALE to CLKOUT	660	–	7 t_{CLCL}-40	–	ns
t_{SHSL}	CLKOUT high time	160	–	2 t_{CLCL}-40	–	ns
t_{SLSH}	CLKOUT low time	960	–	10 t_{CLCL}-40	–	ns
t_{SLLH}	CLKOUT low to ALE high	60	140	t_{CLCL}-40	t_{CLCL}+40	ns

System Clock Timing

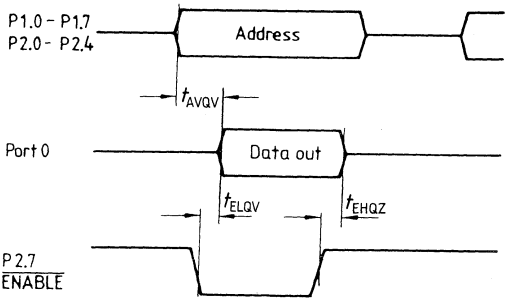


ROM Verification Characteristics

$T_A = 25°C \pm °C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0$ V

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



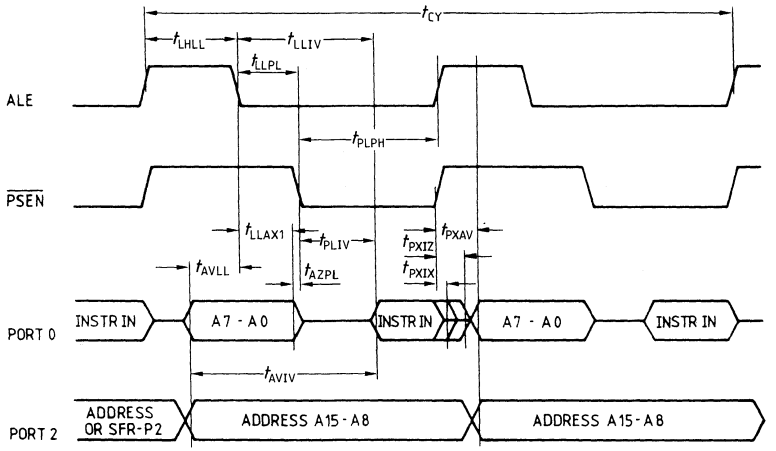
Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

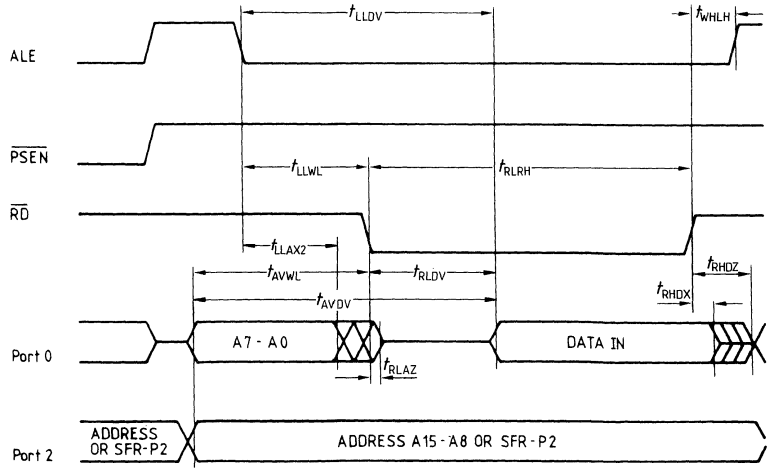
Inputs: P2.5–P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

Waveforms

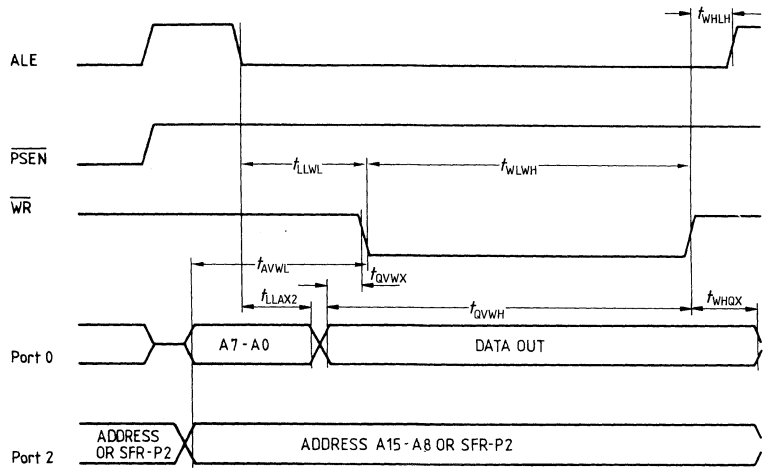
Program Memory Read Cycle



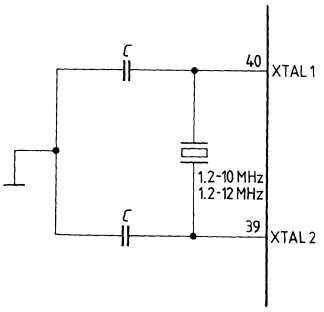
Data Memory Read Cycle



Data Memory Write Cycle

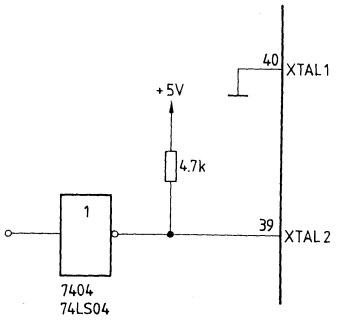


Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

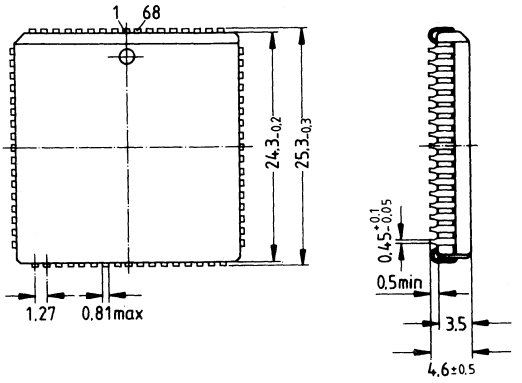
Crystal Oscillator Mode



Driving from External Source

Package Outlines

68-Pin Plastic Leaded Chip Carrier Package, PLCC 68



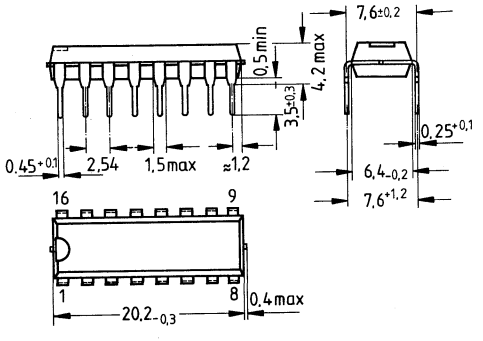
Dimensions in mm

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcomputer
SAB 80515-N-T40/85	Q 67120-C210	with mask-programmable ROM (plastic)
SAB 80535-N-T40/85	Q 67120-C240	for external memory (plastic)
SAB 80515-N-T40/110	Q 67120-C316	with mask-programmable ROM (plastic)
SAB 80535-N-T40/110	Q 67120-C313	for external memory (plastic)

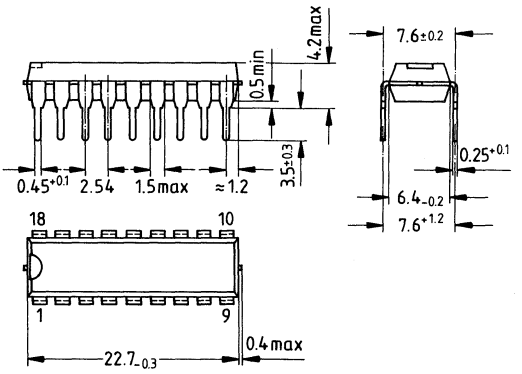
Summary of Package Outlines

Plastic Package, P-DIP-16
(dual-in-line package)
20A16 DIN 41870 T9



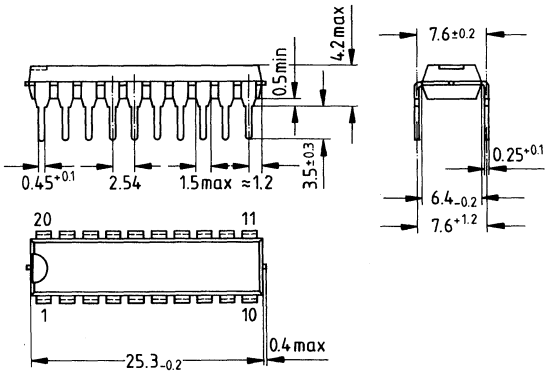
Dimensions in mm

Plastic Package, P-DIP-18
(dual-in-line package)
20A18 DIN 41870 T9



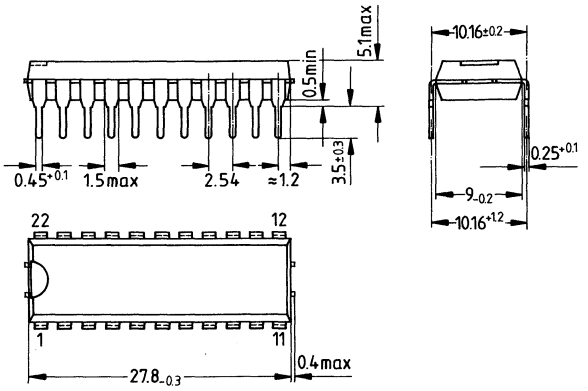
Dimensions in mm

Plastic Package, P-DIP-20
(dual-in-line package)
20A20 DIN 41870 T9



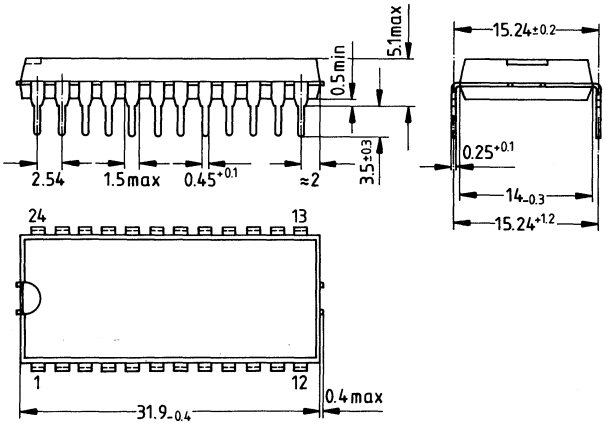
Dimensions in mm

Plastic Package, P-DIP-22
(dual-in-line package)
20D22 DIN 41870 T11



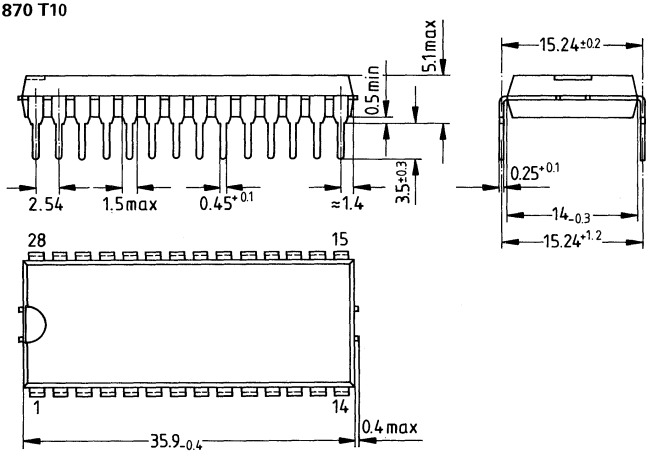
Dimensions in mm

Plastic Package, P-DIP-24
(dual-in-line package)
20B24 DIN 41870 T10



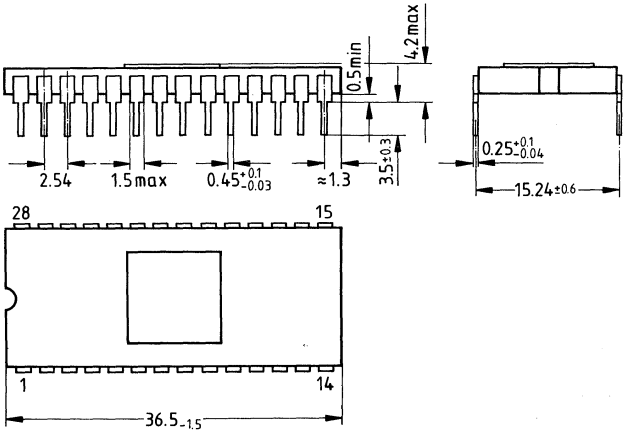
Dimensions in mm

Plastic Package, P-DIP-28
(dual-in-line package)
20B28 DIN 41870 T10



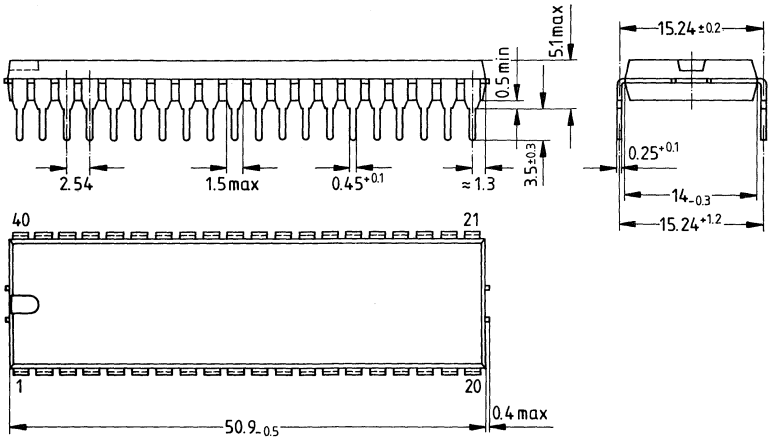
Dimensions in mm

Ceramic Package, C-DIP-28
(dual-in-line package)
20B28 DIN 41870 T10



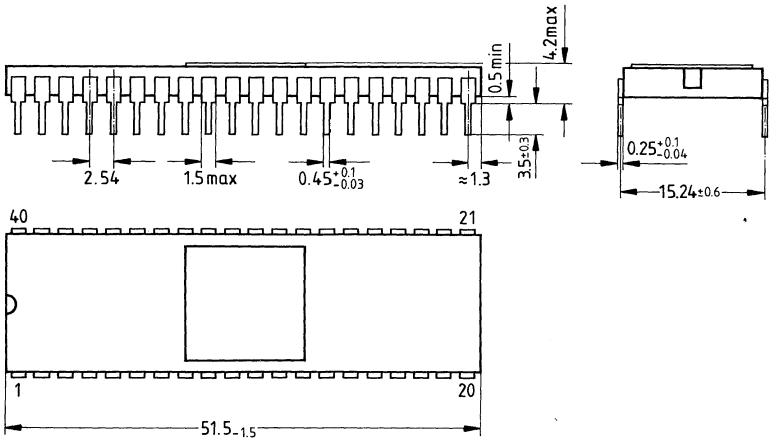
Dimensions in mm

Plastic Package, P-DIP-40
(dual-in-line package)
20B40 DIN 41870 T10



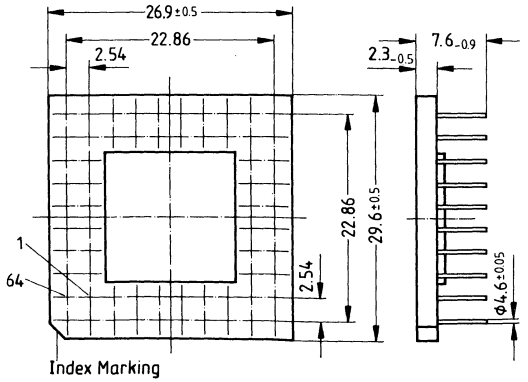
Dimensions in mm

Ceramic Package, C-DIP-40
(dual-in-line package)
20B40 DIN 41870 T10



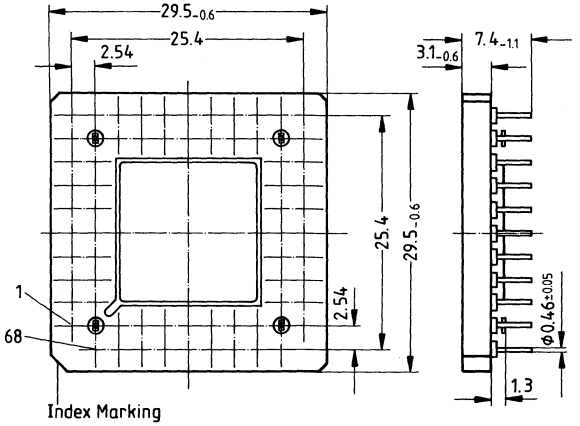
Dimensions in mm

Ceramic Package, C-PGA-64
(pin-grid-array)



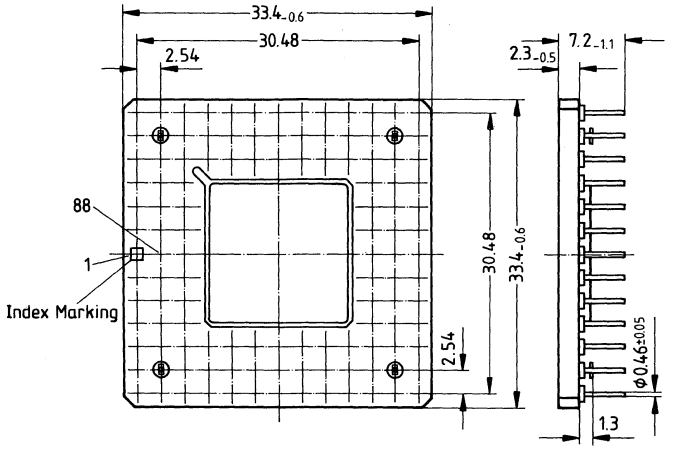
Dimensions in mm

Ceramic Package, C-PGA-68
(pin-grid-array)



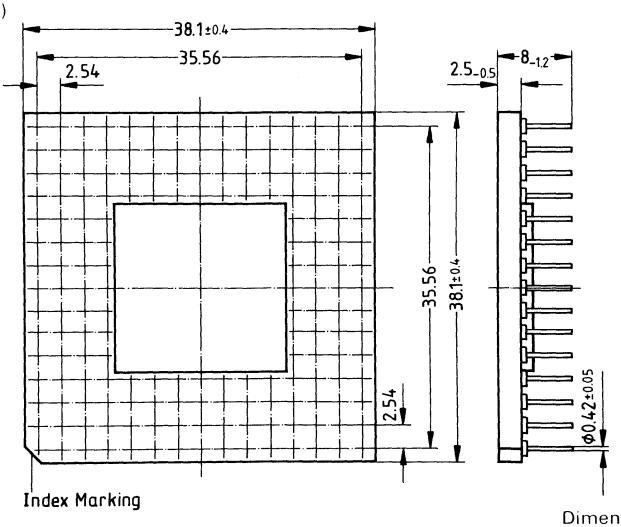
Dimensions in mm

Ceramic Package, C-PGA-88
(pin-grid-array)



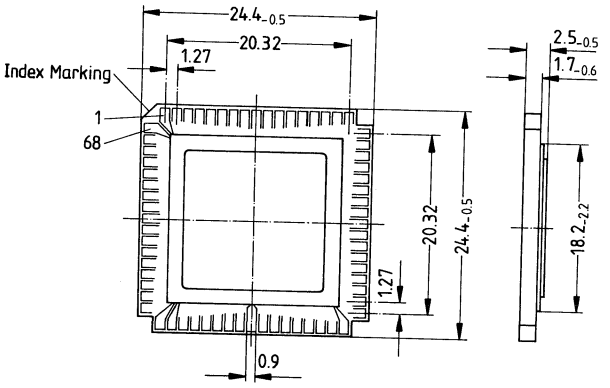
Dimensions in mm

Ceramic Package, C-PGA-145
(pin-grid-array)



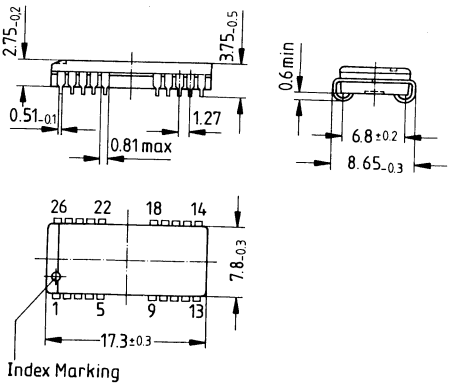
Dimensions in mm

Ceramic Package, C-CC-68
(chip-carrier)



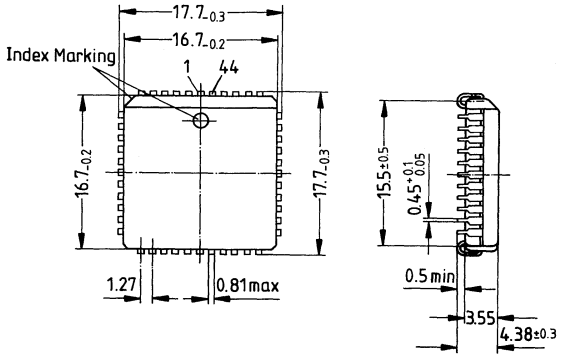
Dimensions in mm

Plastic Package, P-SOJ-26/20
(Plastic small outline J-lead) - **SMD**



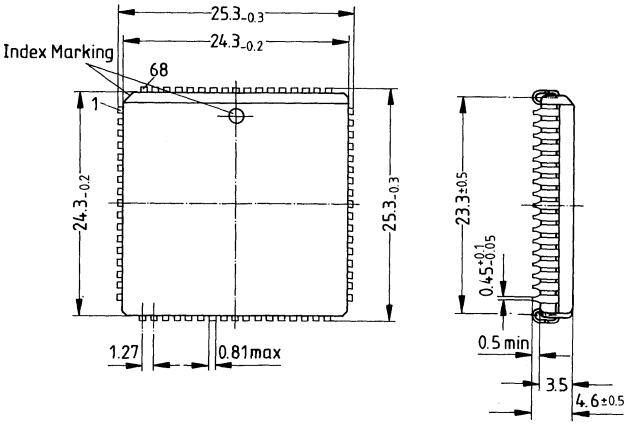
Dimensions in mm

Plastic Package, PL-CC-44
(plastic leaded - chip carrier) - **SMD**



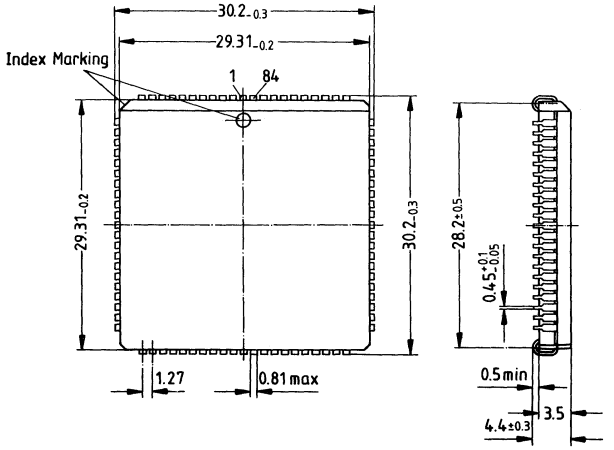
Dimensions in mm

Plastic Package, PL-CC-68
(plastic leaded - chip carrier) - **SMD**



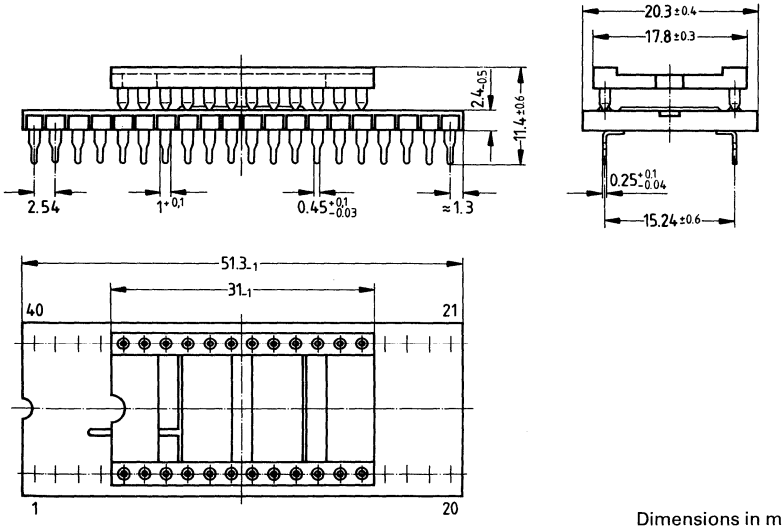
Dimensions in mm

Plastic Package, PL-CC-84
(plastic leaded - chip carrier) - **SMD**



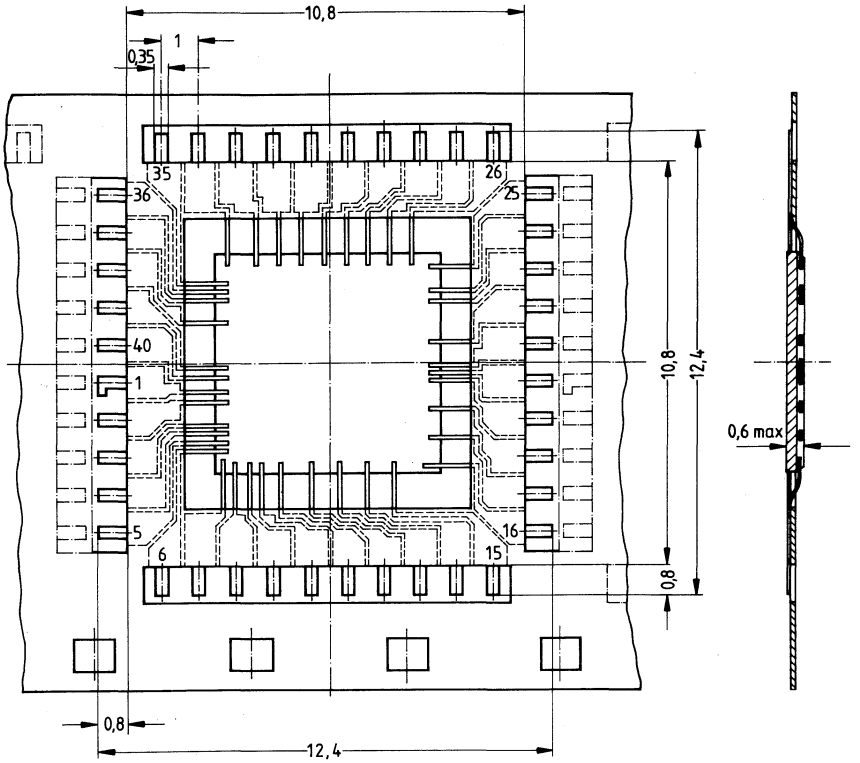
Dimensions in mm

Piggyback



Dimensions in mm

MIKROPACK
16 mm, 40 Pins - SMD



Dimensions in mm

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